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Modulation Technique and Control of DC/AC Inverters with Low Harmonic Distortion
低諧波失真直流/交流逆變器之調制技術與控制

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ABSTRACT

This thesis presents a research on the modulation technique and control of DC/AC inverters with low harmonic distortion. The strategies are applied to the main parts in an inverter, including the power stage and the controller.

A new transient boost technique for the inverter has been proposed for the power stage. This technique can solve the problem of pulse dropping and widen the modulation range, in order to reduce the harmonic distortion at the output to give better input/output reproduction and amplification.

The use of boundary control with second-order switching surface for the control of DC/AC inverters has been proposed for the controller section. The control method is simple and does not require any complicated computation of the system transfer function or control loop compensation. The output voltage can obtain near-optimal response when it is subject to large-signal disturbances or input voltage variation.

With further enhancement in the boundary control scheme, the high-order switching surface of the boundary control for DC/AC inverters has been proposed. The proposed switching surface takes the state variation into consideration, this gives better performance of replication and amplification of the reference signal. The contents of this thesis are as follows.

In Chapter 1, the operational characteristics and limitations of existing DC/AC inverters will be discussed. Then, a survey on various methods for dealing with harmonic distortion will be presented. The methods under investigation can be classified into two main streams, including power stage modulation technique and control of the switching profile.

In Chapter 2, the concept of transient dc-link boost technique will be derived. It is based on increasing the dc link voltage and reducing the modulation index momentarily, when the modulating signal is large. Apart from effectively reducing

harmonic distortion at the output, the proposed method can also widen the dynamic modulation range and thus reduce the required supply voltage. A 10 W prototype with a full-bridge inverter has been built. Some pulses are artificially dropped in the gate signals to simulate the pulse-dropping effect. The inverter output harmonic spectra with and without the transient boost have been compared.

In Chapter 3, the concept of using a second-order switching surface in the boundary control of inverters will be derived. It is based on estimating the state trajectory movement after a switching action, resulting in a high state trajectory velocity along the switching surface. This phenomenon accelerates the trajectory moving toward the target operating point. A 100 W full-bridge inverter has been built. Dynamic responses of the inverter supplying to a resistive load, an inductive load and a diode rectifying circuit have been studied.

In Chapter 4, a generalized high-order switching surface for the boundary control of inverters will be derived. It gives better dynamic control of inverters than the first-order or second-order switching surfaces discussed in chapter 3. As the proposed switching surface is much more close to the ideal switching surface, the trajectory velocity along the switching surface is very high. This makes the trajectory move toward the target operating point in two switching actions during any level of signal disturbance. The proposed control method has been successfully applied to a 300 W full-bridge inverter. The system can revert to the steady state in two switching actions during the any level of signal variations in the input voltage, load disturbances, and output reference.

In Chapter 5, an overall conclusion of the research topics and some suggestions for further research will be given.

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CHAPTER 1

OVERVIEW AND BACKGROUND OF RESEARCH

1.1 Introduction

In recent years, due to the low cost, small in size and high efficiency, pulse-width modulation (PWM) inverters have been employed for various applications, such as, driving motors [Lowery and Petro 1994; Jang and Won 1994; Kim *et al* 2001], uninterruptible power supplies [Chen and Chu 1995; Abdel-Rahim and Quaicoe 1996; Ryan *et al* 1997], even audio power amplifiers [Smith *et al* 1999; Ginart *et al* 2003; Pascual *et al* 2003]. Generally, a single-phase PWM inverter is used in low-power applications. To obtain a high-quality output, the PWM inverter should provide tight output voltage regulation, low total harmonic distortion (THD) and low output impedance against load variations. Thus, harmonic distortion is one of the most crucial topics among various investigations of PWM inverters [Hamman and van der Merwe 1988; Masukawa and Iida 1994; Bowes and Clark 1995]. The nonlinear action of the PWM inverter generates an infinite sequence of Fourier components, the term harmonic distortion or harmonic are usually employed for the description of those unwanted components. Different switching topologies have been proposed to reduce the harmonics, for example, dead time compensation [Sukegawa *et al* 1991; Choi and Sul 1996]; overmodulation control method [Kerkman *et al* 1995]; random PWM switching scheme [Hui *et al* 1997; Covic and Boys 1998], programmed PWM technique [Enjeti *et al* 1990] and space-vector technique [Bowes and Grewal 1999; Bowes and Singh Grewal 2000]

Besides the harmonic problem, dynamic response is also an important issue in the control of inverter [Holtz and Beyer 1993; Jung and Tzou 1993; Dahono and Taryana 2003; Rech and Pinheiro 2004;]. Non-optimal dynamic response will lead to overshoot or undershoot and also pollute the original reference signal profile. Due to

the non-linear nature of inverters, the major reason of non-optimal dynamic response is the linearization of control algorithms which lead to poor resemblance between waveform of the modulating signal and the output waveform under large signal disturbances. Audio power amplifier is one of the examples that the output waveform is always not purely periodic sinusoidal and has large signal transient while playing heavy metal music. For an instant large modulating signal change, for example a heavy bass drum kick, the inverter may reproduce that signal incorrectly with distortions. Thus, non-optimum transient responses such as overshoot, undershoot or oscillation situations may be occurred.

In this thesis, from the power stage point of view, a transient dc-link boost technique to avoid pulse dropping in digital amplifiers will be introduced. This idea aims to reduce the harmonic distortion when facing the situation of pulse dropping. From the controller point of view, a boundary control with second- and high-order switching surfaces for inverters will also be investigated. These ideas aim to optimize the transient response under large signal disturbance with good steady state performance and low harmonic distortion.

1.2 Harmonic distortion due to Pulse-Dropping

1.2.1 PWM inverter with Dead time

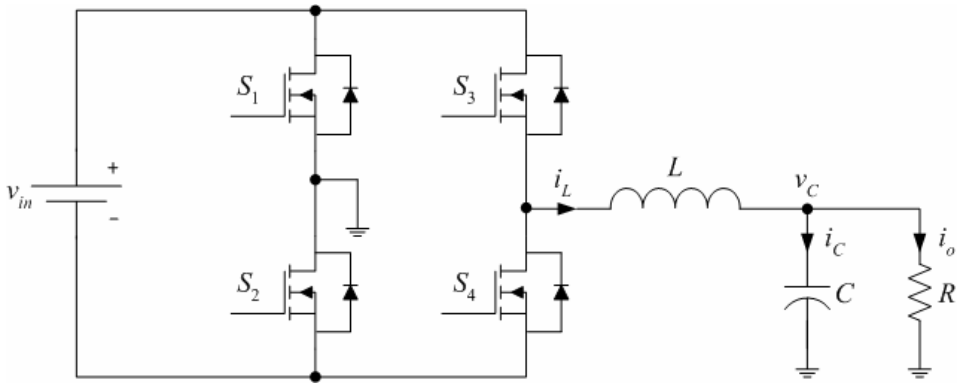


Fig. 1.1 Typical configuration of H-bridge inverter.

In practice, the switches of the H-bridge inverter are driven to be on and off, then the output voltage will change between positive and negative correspondingly. Fig.1.1 shows a typical H-bridge inverter configuration which comprises of a dc voltage source, four switches, an LC filter and a load. In the transition time when high side switching S_1 switched on, the low side switch S_2 should be off correspondingly. However, due to the limited response time and delay time of the switches, these two switches may be switched on simultaneously, then shoot-through will occur and the switches may be impaired due to high short-circuit current. Thus, dead time is introduced in order to avoid cross-talk within the switches. In fact, the addition of dead time in the driving signal can prevent shoot-through. However, the instability and harmonic distortion problems are also arisen [Ueda *et al* 1989; Wu *et al* 1999], and therefore many different dead time compensation methods were proposed for dealing with those problems [Dodson *et al* 1990; Jeong and Park 1991; Leggate and Kerkman 1997; Munoz and Lipo 1999; Cichowski and Nieznanski 2005]

1.2.2 Pulse-dropping in class D audio amplifiers

PWM inverter has found numerous applications in both industry and domestic market. In particular, owing to the high fidelity, efficiency and rapid development in digital audio technology, PWM inverter becomes popular in audio power amplifier designs [Hlorns and Sandler 1993; Floros and Mourjopoulos 1999; Lau *et al* 1999; Lau *et al* 2000]. It is also called class D audio amplifier. For typical class D analog switching amplifier, the sinusoidal modulating signal is compared with a high frequency triangular wave or saw-tooth, and then the compared output signal drives the full-bridge inverter for the amplification. [Mohan *et al* 1995] For the digital class-D audio amplification, Pulse Code Modulation (PCM) is used instead of the sinusoidal reference signal for the generation of PWM [Pascual *et al* 2003]. Microprocessor or Field-

Programmable Gate Arrays (FPGA) is used to decode the PCM and convert to PWM signal. Most common sampling frequeny the analog signal is 44.1kHz, and in order to reproduce the audio signal with high-fidelity, an eight-time oversampling will usually be applied to the PCM audio signal and the resultant sampling frequency becomes 352 kHz. The oversampled PCM data will be converted to PWM format to drive a high power H-bridge circuit. One of the important considerations in designing digital audio power amplifiers is the switching characteristics of the gate drivers and power devices. It is well known that the higher is the power rating of the device, the slower is the switching response. Thus a 352 kHz switching frequency is too high for high power applications, due to the gate input capacitance, output capacitance, finite rise time and fall time of the semiconductor switches [Attwood 1983]. These intrinsic parameters limit the minimum pulse width in the output wave form, and thus the maximum modulation index is confined. Generally, with the slight dynamic variation of the reference signal, the modulation range is small. However, the modulation range can be widened under large reference signal variation, which introduces high modulation index. A high value of modulation index will make the pulse width of the gate signals narrow. Nevertheless, dead time is also exist in between those narrow pulses, making the pulses becomes narrower. Thus, due to the intrinsic capacitance and resistance, the turn on and off response time of the switches are limited, the narrow pulses cannot be retrieved at the output of the H-bridge and the corresponding effects on the load are lost, thus pulse-dropping appears. This scenario will conclude in the generation of odd harmonics in the output. Thus, the maximum modulation index used in many designs is usually to be between 0.1 and 0.2 in order not to operate the switches at the crucial region. Hence, the modulation range is not fully utilized and the required supply voltage level is higher than the one operating with a wider modulation range under the same output power.

1.3 Boundary Control of inverters

1.3.1 Boundary Control

Boundary control was firstly introduced for power electronics application in [Burns and Wilson 1976]. It is a geometric based control technique [Greuel *et al* 1997] or one type of variable structure controls [DeCarlo *et al* 1988; Hung *et al* 1993] for switching power converters. On the other hand, it is targeted for large-signal control algorithm which addresses the complete operation of a converter and does not separate start-up, steady state, and transient modes. [Krein 1998].

A boundary is a switching surface which is used to bisect the state plane into two regions, and the converter will switch back and forth between on- and off-state circuit topologies. For the state-plane, it is formed by the state trajectories which are obtained from the state equations of the converter. The dimension of state plane is equal to the number of state variable in the systems and the number of switching combination determines the number of trajectory families [Malesani *et al* 1995; Oppenheimer *et al* 1996]. For typical two-state dc-dc converters, the trajectories are either spirals or hyperbolae and one family of trajectories will not intersect with each other except at the point of equilibrium. Typical state-trajectory families of an inverter are shown in Fig. 1.2.

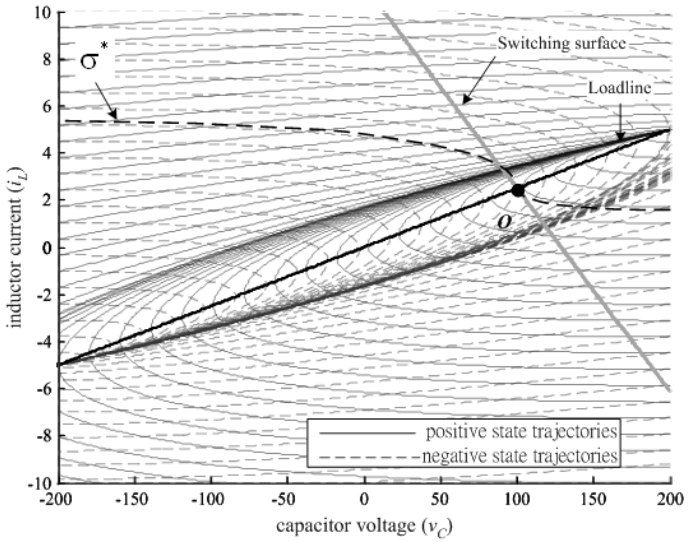


Fig. 1.2 State-trajectory families of an inverter.

Points along switching surface can be classified into refractive, reflective, and rejective, these three possibilities are shown in Fig. 1.3 [Krein 1998].

1. The points which one side of state trajectory is driven towards and the other side is driven out from the switching surface are called refractive points. Voltage hysteresis control is one of the examples in which a vertical voltage switching surface is used to control a buck converter. By comparing the distance of any pair of two successor points which are defined as every subsequent point of switch action along the switching surface, the stability in this region can be resolved [Munzert and Krein 1996].

2. The points which both sides of state trajectory are driven towards the switching surface are called reflective points. Any operation in these points is called sliding mode operation. Converters with sliding mode control has been well-investigated for many years [Carpita and Marchesoni 1996; Morel *et al* 2002; Ahmed *et al* 2003; Perry *et al* 2004]. Due to the specific sliding behavior, the state of the converter will move along the switching surface until it reaches the target operating point unless it is forced to change its target operating point such as reference change or load-disturbance occurrences.

3. The points which both sides of state trajectory are driven out from the switching surface are called rejective points. If the state reaches these points, no further switching action can compel the state to move toward the boundary. Therefore the state trajectory will follow its own natural movement without any control applicability, and the state becomes uncontrollable. In fact, converter should not operate in the region with rejective points otherwise the system would become unstable.

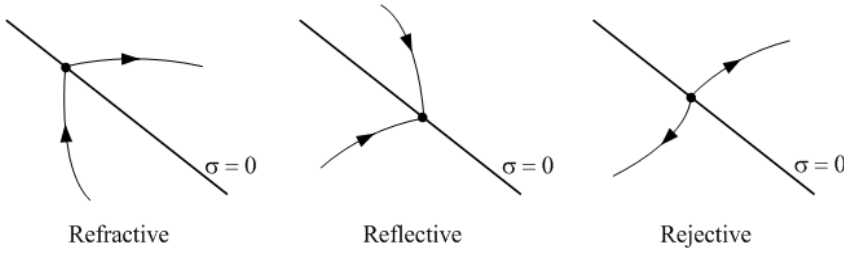


Fig. 1.3 Trajectory Behaviors along the switching surface.

In [Bass and Krein 1990], for the boundary control of inverter, a family of elliptic asymptotic surfaces will be obtained on the state plane, and its shape will vary with the amplitude and frequency of the sinusoidal reference [Bass and Krein 1989]. Therefore by selecting a suitable switching surface for the boundary control, the inverter can automatically generate a desired sinusoidal output without any reference signal [Biel *et al* 2001; Biel *et al* 2004]. Various boundary control techniques such as sliding-mode control [Silva 1992; Malesani *et al* 1996a] and hysteresis control [Kato and Miyao 1988; Jung *et al* 2002] are commonly employed in controlling power inverters

1.3.2 Ideal Switching Surface

Typical switching surface is a linear one (σ^1). Various σ^1-derived boundary control methods, such as the sliding-mode control and hysteresis control, are widely studied for power converter [Greuel *et al* 1997; Biel *et al* 2001; Ramos *et al* 2003; Filho and Perin 1997]. All these methods provide good steady-state and large-signal response and stability, but the transient dynamics is still non-optimal. Much research work extends the concepts, such as the adaptive hysteresis control in [Nguyen and Lee 1995; Tan *et al* 2004], to enhance the dynamics response.

In order to achieve optimum dynamic response and global stability, an *ideal switching surface* (σ^*) should be engaged for the boundary control which shown in Fig. 1.2. It is a surface which moves along the only on- and off-state trajectory through the target operating point. It was firstly proposed in 1977 [Burn and Wilson 1977; Huffman *et al* 1977]. Due to the high complexity of the control implementation, a near-optimum controlling method using feedforward of output current and input voltage with current-mode control was proposed in order to reduce its complexity [Redl and Sokal 1986]. In addition, an exact ideal switching surface with optimum dynamic can be obtained by solving the eigenvalues of system state equations [Biel *et al* 1996; Biel *et al* 1998].

However, these proposed switching surfaces require sophisticated computation which is difficult to be implemented by analog circuitry. Therefore, some approximations are employed in these implementations. Recently, boundary control using second-order switching surface (σ^2) was proposed in [Leung and Chung 2004] that the dynamic behaviors are better than σ^1. By approximating the ideal switching surface with a second order function, σ^2 can achieve near-optimum large-signal response with simple implementation of the control circuit.

1.4 Organization of the Thesis

The thesis contains five chapters. *Chapter 2* presents the concept of transient dc-link boost technique. It is based on increasing the dc link voltage and reducing the modulation index momentarily when the modulating signal is large. Apart from effectively reducing harmonic distortion at the output, the proposed method can also widen the dynamic modulation range and thus reduce the required supply voltage. Theoretical and experimental analysis will be performed accordingly.

Chapter 3 presents the concept of using a second-order switching surface in the boundary control of inverters. By estimating the state trajectory movement after a switching action, a high state trajectory velocity along the switching surface can be obtained. This phenomenon accelerates the trajectory moving toward the target operating point. Dynamic responses of the inverter supplying to a resistive load, an inductive load and a diode rectifying circuit are studied.

Chapter 4 presents the concept of using high-order switching surface (σ^N) for boundary control of inverters. Comparing with the first-order (σ^1) and recently proposed second-order (σ^2) switching surfaces, the inverter with σ^N exhibits better dynamic responses. The comparison among σ^1, σ^2 and σ^N will be presented. The parametric sensitivity and large-signal characteristics of the inverter will also be

discussed. The proposed control method has been successfully applied to a 300W, 110V, 60Hz, single-phase full-bridge inverter. The steady-state and large-signal dynamic behaviors of the inverter supplying to resistive and nonlinear inductive loads will be given accordingly.

Chapter 5 concludes the thesis, together with concise discussions on further research.

CHAPTER 2

TRANSIENT DC-LINK BOOST TECHNIQUE OF PWM INVERTER CONTROL FOR ELIMINATING PULSE-DROPPING DISTORTION

2.1 Introduction

This chapter presents a transient dc-link boost technique to avoid pulse dropping in digital amplifiers. The concept is based on boosting the dc link voltage and reducing the modulation index momentarily, when the modulating signal is large. Apart from lowering harmonic distortion at the output, the method can also widen the dynamic modulation range and reduce the required supply voltage. A 10W prototype has been built. Some pulses are artificially dropped in the gate signals for simulating the pulse-dropping effect. The output harmonic spectra of the prototype with and without the transient boost have been compared.

2.2 Mathematical Analysis

2.2.1 Relationships among the supply voltage, modulation index, and minimum pulse width

Narrow pulses appear when the modulating signal v_m is at the maximum or minimum. Consider a switching cycle shown in Fig. 2.1, when v_m is at the maximum. The average voltage $\hat{v}_o$ of the pulse is equal to

$$\hat{v}_o = (2d - 1) V_d \quad \Rightarrow \quad d = \frac{1}{2}(1 + M) \tag{2.1}$$

where $d = t_1 / T$ is the ratio of the duration of the pulse at the positive value (i.e., t_1) to the period T, V_d is the dc link voltage, and $M = \hat{v}_o / V_d$ is the modulation index.

Thus, the minimum pulse duration $t_{\min}$ is equal to

$$t_{\min} = [1 - \frac{1}{2}(1 + M)]\, T = \frac{1}{2}(1 - M)\, T \tag{2.2}$$

$t_{\min}$ decreases as M increases, giving the required minimum response time of the devices. If the switch cannot respond to $t_{\min,}$ pulse dropping occurs. For a given output power, a feasible way of reducing M is to increase V_d. Based on (2.2), the ratio of increment in $t_{\min}$ to the ratio of increment in V_d is

$$\phi = \frac{t_{\min,2}}{t_{\min,1}} = \frac{1 - M_1 / \Psi}{1 - M_1} \tag{2.3}$$

where $\Psi = V_{d,2} / V_{d,1}$, M_1 is the modulation index when the supply voltage is $V_{d,1}$, $t_{\min,2}$ is the minimum pulse duration when the supply voltage is $V_{d,2}$. Fig. 2.2 shows the relationships between ϕ and Ψ. Significant increment in ϕ appears, when Ψ is between 1 and 3.

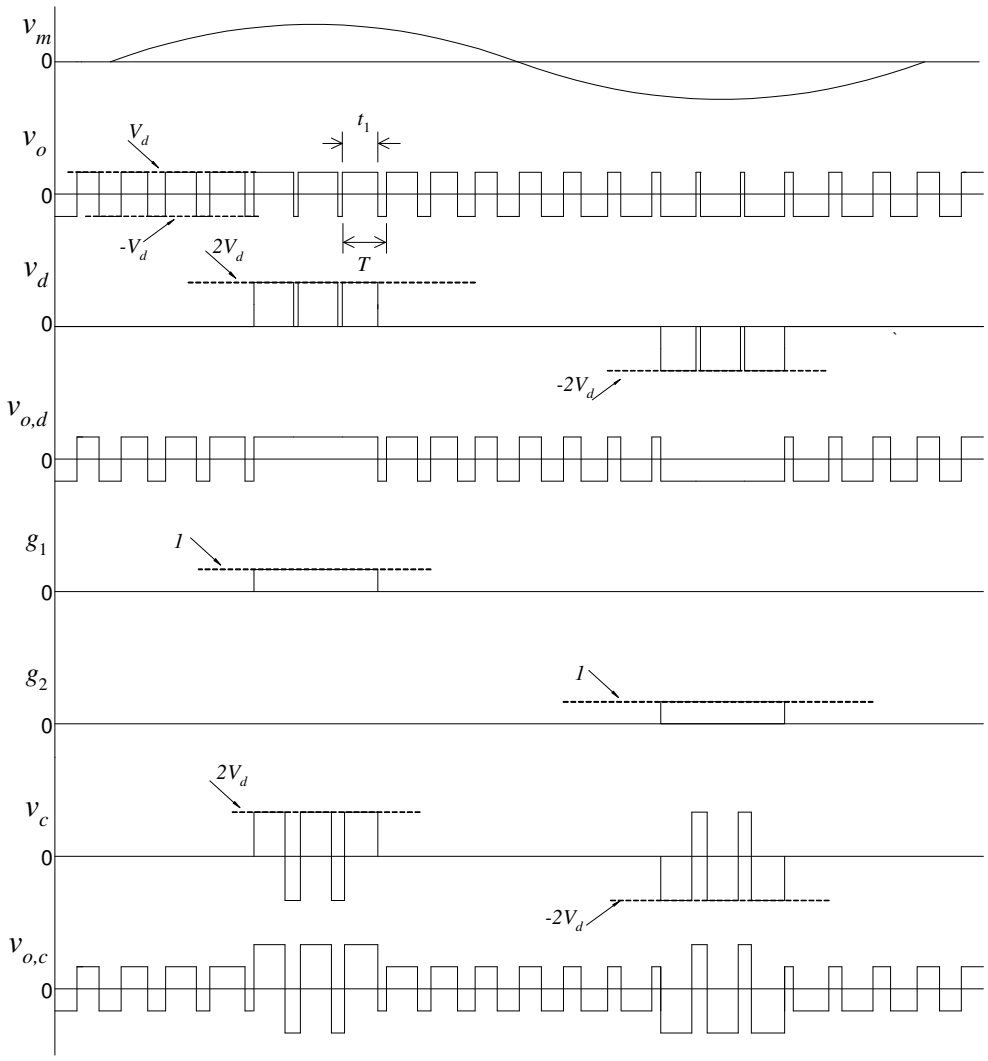


Fig. 2.1 Waveforms of v_m , v_o , v_d , $v_{o,d}$, g_1 , g_2 , v_c , and $v_{o,c}$.

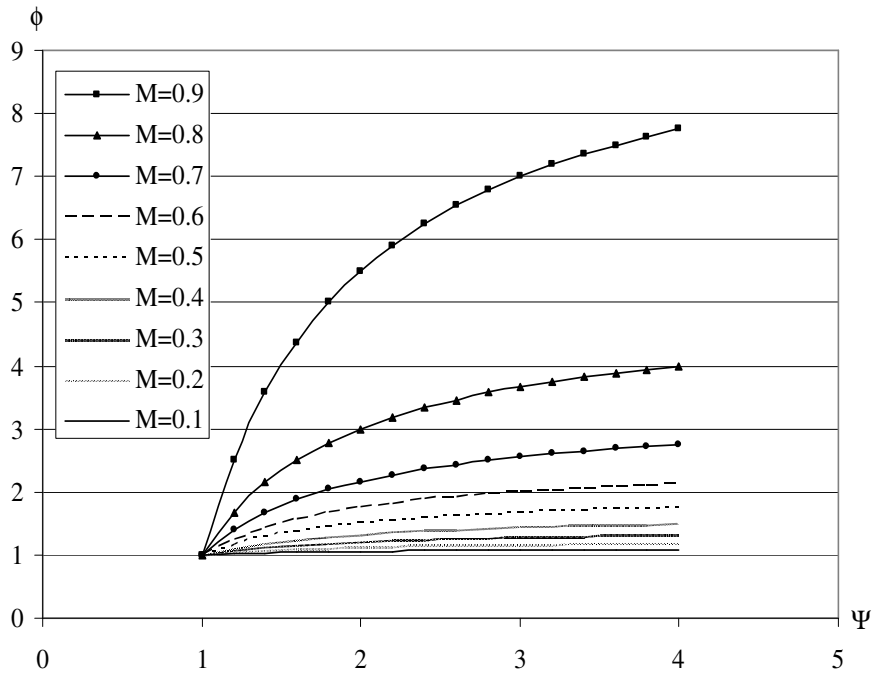


Fig. 2.2 Relationships between ϕ and Ψ.

2.2.2 Harmonic spectra of the output

Fig. 2.1 shows the ideal output waveform v_o and the one with dropped pulses $v_{o,d}$. By the using the similar approach in [Zhou *et al* 2004], the spectral function of v_o is

$$\begin{aligned} v_o(t) &= F(\omega_c t, \omega_v t) \\ &= V_d \ M \ \cos(\omega_v t) + A(t) \end{aligned} \tag{2.4}$$

where ω_c is the switching frequency and ω_v is the modulating signal frequency,

$$\begin{aligned} A(t) = &\sum_{m=1}^{\infty} \frac{4V_d}{m\pi} \sin\frac{m\pi}{2} J_0(\frac{m\pi M}{2}) \cos(m\omega_c t) \\ &+ \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{4V_d}{m\pi} \sin\frac{(m+n)\pi}{2} J_n(\frac{\pi m M}{2}) \cos(m\omega_c t + n\omega_v t) \end{aligned}$$

$v_{o,d}$ is derived by superimposing $v_o(t)$ and $v_d(t)$ in Fig. 2.1,

$$v_{o,d}(t) = v_o(t) - v_d(t) \tag{2.5}$$

where $v_d(t) = v_o(t)[g_1(t) + g_2(t)] - V_d\,[g_1(t) - g_2(t)]$.

The spectral function of $v_{o,d}(t)$ can be obtained by (2.4) and (2.5), in which $g_1(t)$ and $g_2(t)$ can be expressed as

$$g_1(t) = \frac{\theta}{2\pi} + \sum_{k=1}^{\infty} \frac{2\sin(k\theta/2)}{k\pi} \cos(k\omega_v t) \tag{2.6}$$

$$g_2(t) = g_1(t + \frac{\pi}{\omega_v}) \tag{2.7}$$

where θ is the angular duration of the pulse dropping.

$g_1(t)$ and $g_2(t)$ generate harmonics of significant amplitude, which is due to the multiplication of V_d and $g_1(t)$ and $g_2(t)$. $t_{\min}$ can be effectively increased if V_d is increased. The proposed method momentarily double the supply voltage and reduce M by half, if the estimated pulse width is too narrow that pulse dropping may happen. The waveform becomes

$$\begin{aligned} v_{o,c}(t) &= v_o(t)[1 - g_1(t) - g_2(t)] + v_c(t)[g_1(t) + g_2(t)] \\ &= v_o(t) + [B(t) - A(t)][g_1(t) + g_2(t)] \end{aligned} \tag{2.8}$$

where $v_c(t)$ is the waveform having a magnitude of $2V_d$ and modulation index of M / 2. $v_c(t)$ can be expressed as

$$v_c(t) = V_d \; M \; \cos(\omega_v t) + B(t) \tag{2.9}$$

where

$$\begin{aligned} B(t) = &\sum_{m=1}^{\infty} \frac{8V_d}{m\pi} \sin\frac{m\pi}{2} J_0(\frac{m\pi M}{4}) \cos(m\omega_c t) \\ &+ \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{8V_d}{m\pi} \sin\frac{(m+n)\pi}{2} J_n(\frac{m\pi M}{4}) \cos(m\omega_c t + n\omega_v t) \end{aligned}$$

Eq. (2.4) shows the spectral characteristics of ideal waveform. As shown in eq. (2.5), $v_d(t)$ will introduce considerable harmonic components at the output. Compared with (2.8), the product term $[B(t) - A(t)]$ $[g_1(t) + g_2(t)]$ significantly reduce the harmonic components due to inter-modulation. The frequencies with significant amplitude are just inside the high-order band (>300kHz), so it can be filter out by the low pass filter and the signal can retain high spectral behavior.

2.3 Prototype

An experimental prototype has been built. Fig. 2.3 shows the schematic of the prototype. The component values are tabulated in Table 2.1. For the sake of simplicity, two dc supply sources that provide 5V and 10V are used to achieve the transient boost function. The audio digital code is generated from a CD player. The audio data represents a 1kHz pure sinusoidal signal. A digital audio interface receiver CS 8412 converts the data to PCM code. The PCM code is supplied to a Field Programmable Gate Arrays (FPGA) MAX 9400 for voltage transformation and fed to digital audio PWM processor TAS 5000 to generate PWM signals for the switches. The FPGA will generate two sets of PCM coding and two corresponding sets of PWM signals will be generated by the two PWM processors in Fig. 2.3. The first set is a normal PWM signal with the original modulation index, while the second one is a modified PWM signal with the modulation index reduced by half. The FPGA will estimate the possible width of the pulse generated by the PWM processor. If the estimated pulse width is sufficiently wide, the boost function will not be activated. The first set of PWM signal will be used to drive the switches S_1 to S_4. Conversely, if the pulse width is too narrow (i.e., pulse dropping may occur), the FPGA will generate signals to the multiplexer to select the second set of PWM signal for the switches, as well as the switch S_d to double the dc-link voltage.

Fig. 2.4(a) shows the output waveform without pulse dropping, Fig. 2.4(b) shows the waveform with pulse dropping, and Fig. 2.4(c) shows the waveform with the transient boost. As circled in Fig. 2.4(b), the waveform is distorted and suddenly increased at the peak and valley due to pulse droppings. With the proposed transient boost [Fig. 2.4(c)], the original waveform can be reconstructed, as compared with Fig. 2.4(a). A microscopic investigation into the waveforms is shown in Fig. 2.5. Pulse dropping causes more energy than required transferring to the load. This will thus

increase the instantaneous value of the output [Fig. 2.5(a)]. With the transient boost, the dc link voltage is changed from 5V to 10V and *M* is halved [Fig. 2.5(b)]. As circled in Fig. 2.5(b), the neighborhood pulses are compared during the transient boost. The pulse width is increased. The total energy transferred to the load in the switching cycle is same as the one without pulse dropping.

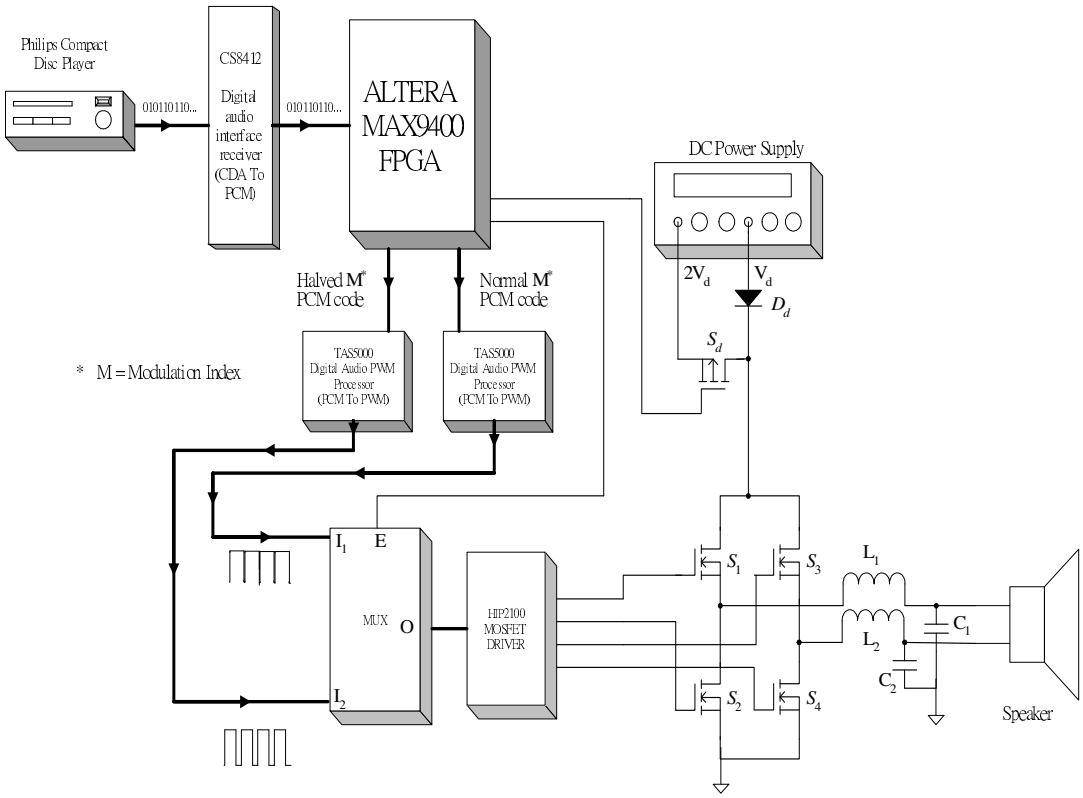
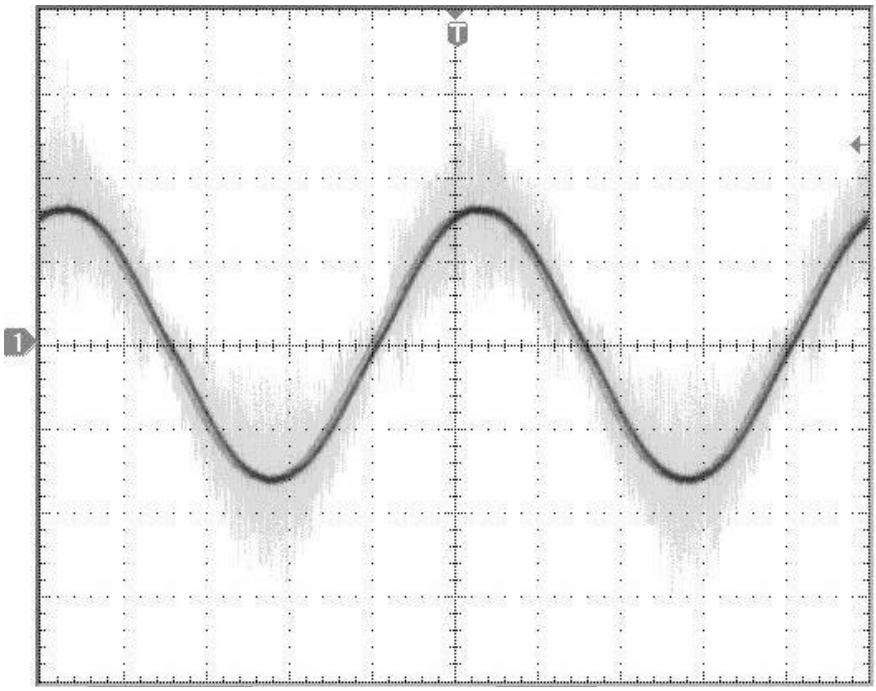
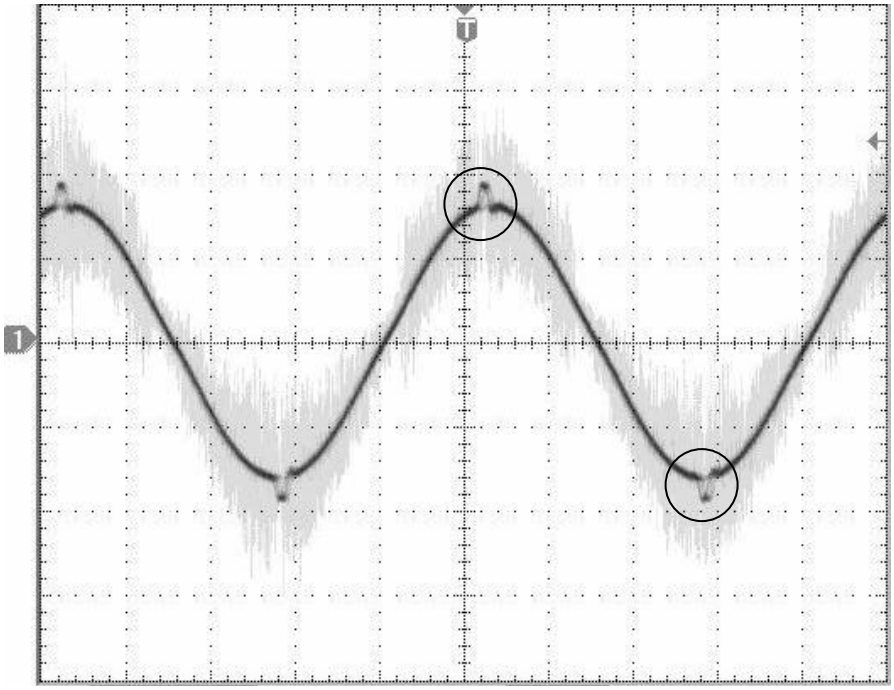


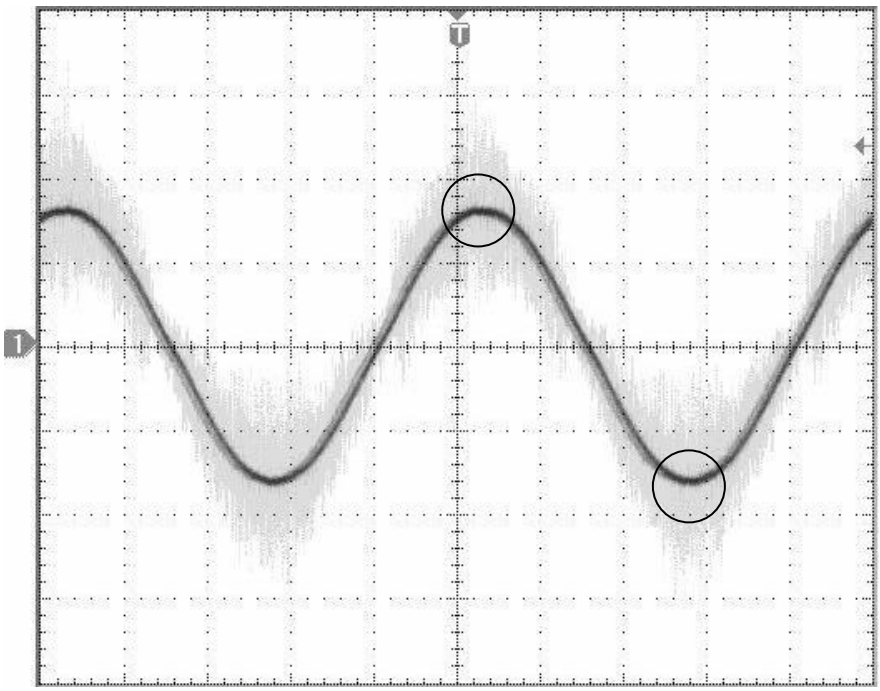
Fig. 2.3 Schematic of the prototype.



(a) Without pulse dropping.

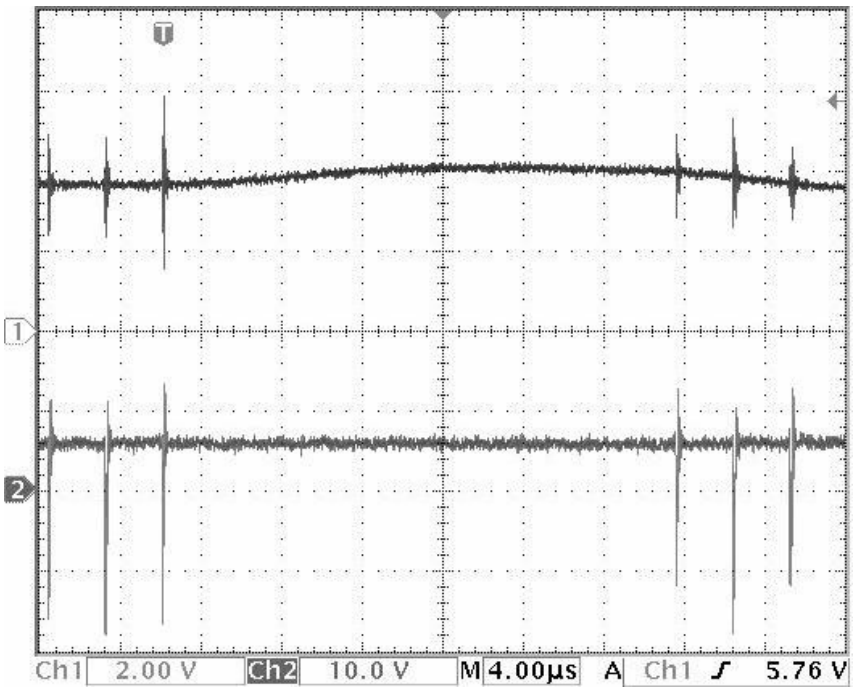


(b) With pulse dropping and without transient boost.

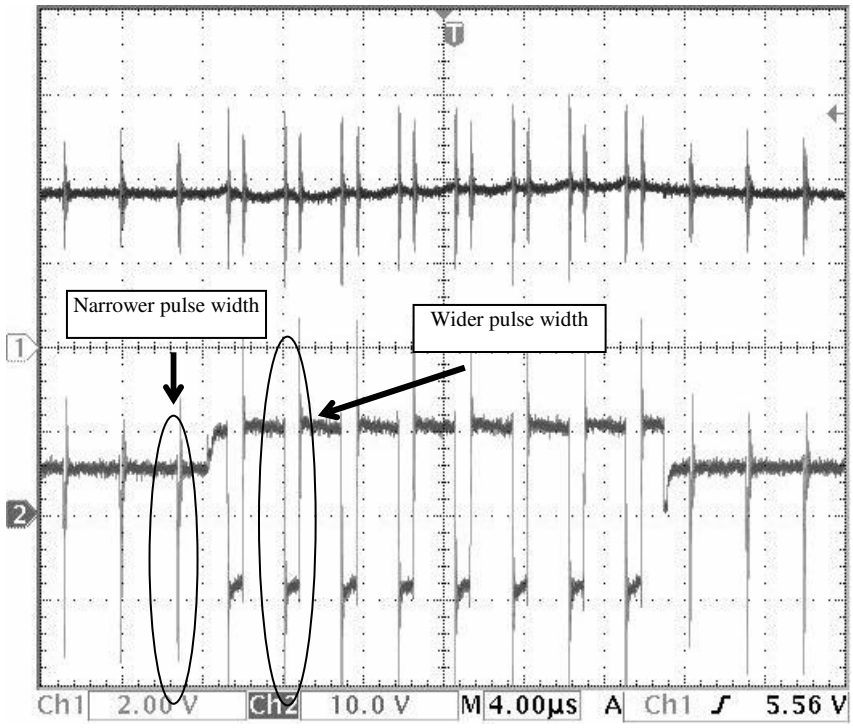


(c) With pulse dropping and transient boost.

Fig. 2.4 Comparisons of the output waveforms (Ch. 1: Output voltage after filtering. Timebase: 200μs/div, 2V/div).



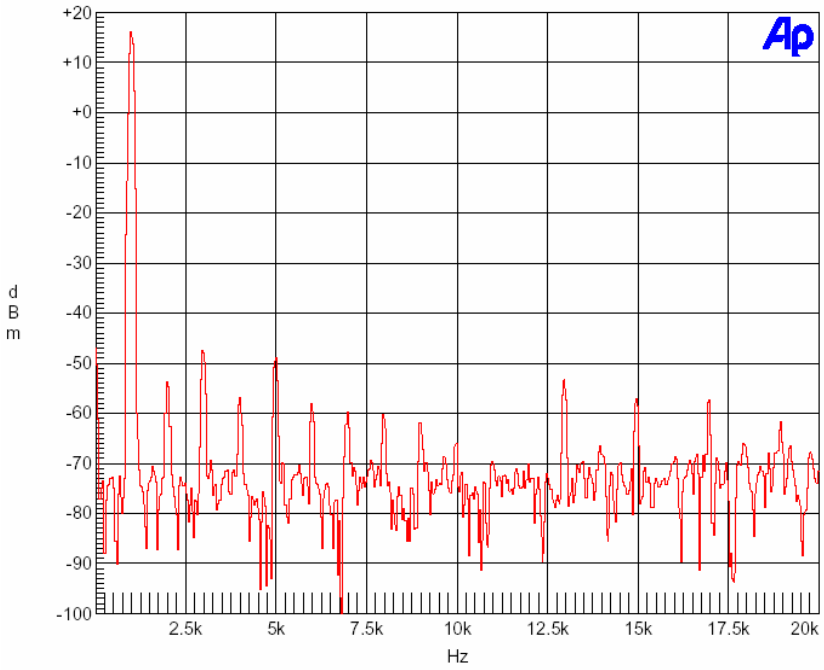
(a) With pulse dropping and without transient boost.



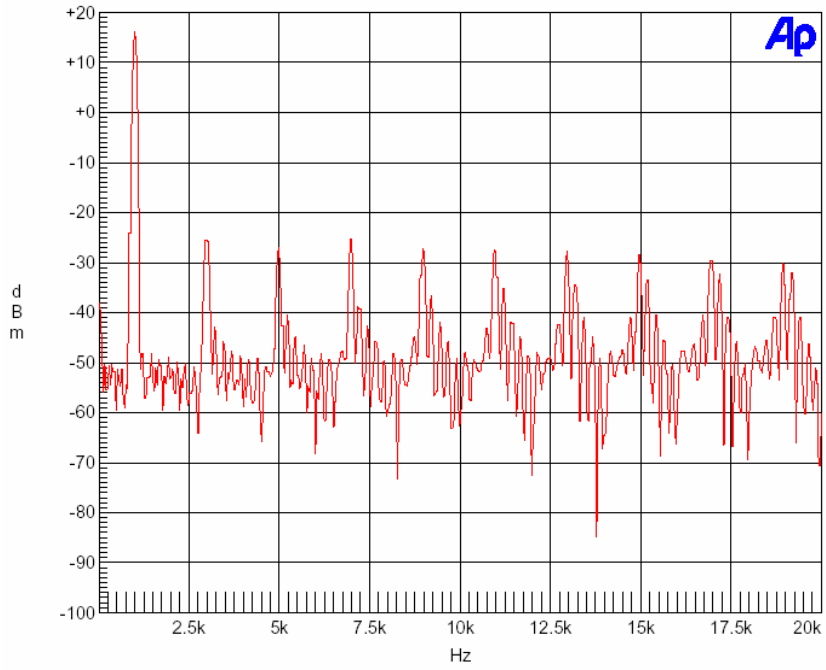
(b) With pulse dropping and with transient boost.

Fig. 2.5 Microscopic study of the two operations. [Ch. 1: Output Voltage after filtering (2 V/div), Ch. 2: Output Voltage before filtering (10 V/div)].

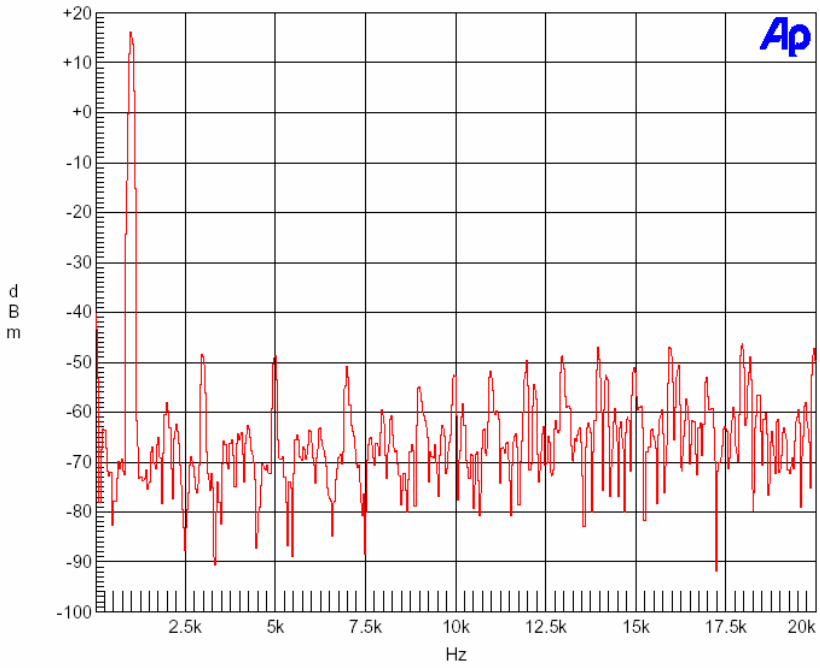
Fig. 2.6 shows the harmonic spectra of the original signal [Fig. 2.6(a)], with pulse dropping [Fig. 2.6(b)], and with the transient boost [Fig. 2.6(c)]. Compared Fig. 2.6(a) with Fig. 2.6(b), the noise level is increased by almost 30dB, due to the pulse dropping effect. With the transient boost [Fig. 2.6(c)], the harmonic spectrum can almost be recovered, demonstrating the effectiveness of the proposed method.



(a) Without pulse dropping.



(b) With pulse dropping and without transient boost.



(c) With pulse dropping and with transient boost.

Fig. 2.6 Comparisons of the harmonic spectra.

Table 2.1 Component values of the prototype

S_1 , S_2 , S_3 , S_4	IRL520N
L_1 , L_2	10 μ H
C_1 , C_2	2.2 μ F
S_d	IRF9630
D_d	1N4001
Impedance of the speaker	6 Ω

2.4 Chapter Summary

A new transient boost technique for digital amplifiers has been proposed. It can solve the problem of pulse dropping and widen the modulation range. Apart from effectively reducing harmonic distortion at the output, the proposed method can also

widen the dynamic modulation range and thus reduce the required supply voltage. The effectiveness of the method has been supported by experimental measurements.

CHAPTER 3

USE OF THE SECOND-ORDER SWITCHING SURFACE IN THE BOUNDARY CONTROL OF INVERTERS

3.1 Introduction

This chapter presents a concept of using a second-order switching surface in the boundary control of inverters. The switching surface is formulated by estimating the state trajectory movement after a switching action. It results in a high state trajectory velocity along the switching surface. This phenomenon accelerates the trajectory moving towards the target operating point. Time-domain responses of the inverter with the proposed boundary control method under large-signal variations have been analyzed. The proposed control scheme has been successfully applied to a 100 W full-bridge inverter. Practical implementation of the system will be given. Dynamic responses of the inverter supplying to different kinds of loads, including a resistive load, an inductive load, and a diode-capacitor rectifying circuit, have been studied. Experimental results show that the inverter output voltage can attain a low total harmonic distortion at different load conditions and fast response to a large-signal load disturbance and an output reference voltage change.

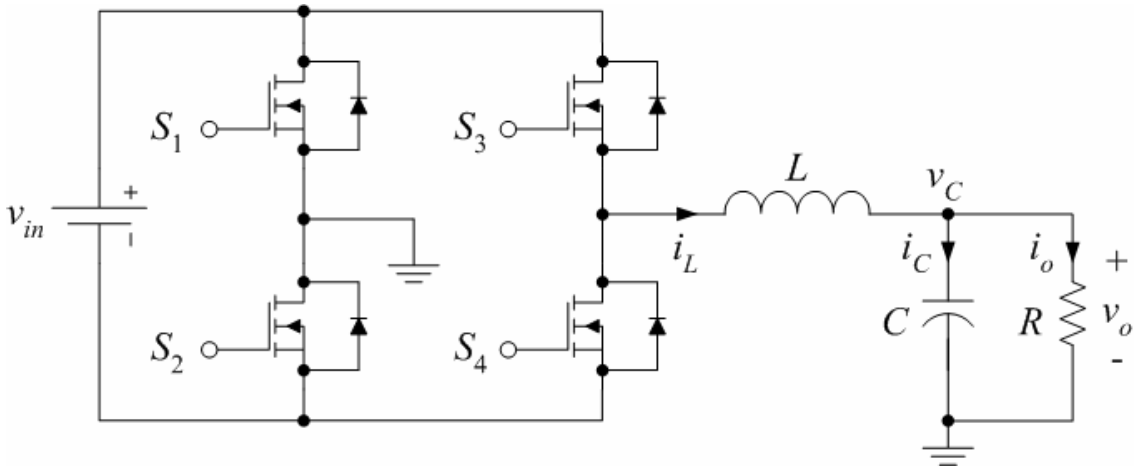


Fig. 3.1 Circuit schematic of typical full-bridge dc-ac inverter.

3.2 Principle of Operation

Fig. 3.1 shows a single-phase full-bridge dc-ac inverter. The inverter is supplied from a dc source v_{in} through a low-pass filter formed by L and C. The load is represented by a resistor R. Switches (S_2, S_3) are switched in anti-phase with (S_1, S_4). The system can be represented by the following state-space equations,

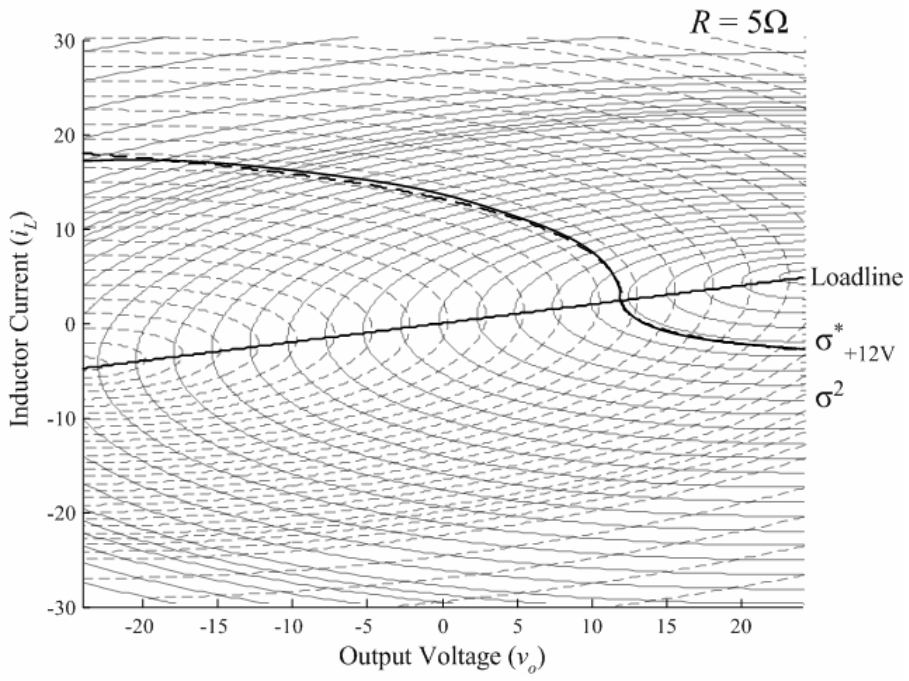
$$\dot{x} = A_0 x + B_0 u + (A_1 x + B_1 u) q_1 + (A_2 x + B_2 u) q_2 \tag{3.1}$$

where $x = [i_L \quad v_C]$, $u = v_{in}$, A_n and B_n are constant matrix and q_i represents the state of the switches. (S_2, S_3) are on if $\{q_1, q_2\} = \{1, 0\}$, and (S_1, S_4) are on if $\{q_1, q_2\} = \{0, 1\}$. Matrices A_0, B_0, A_1, B_1, A_2, and B_2 are defined as $A_0 = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$, $B_0 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$, $A_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$, $B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}$, $A_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$, $B_2 = \begin{bmatrix} -1/L \\ 0 \end{bmatrix}$.

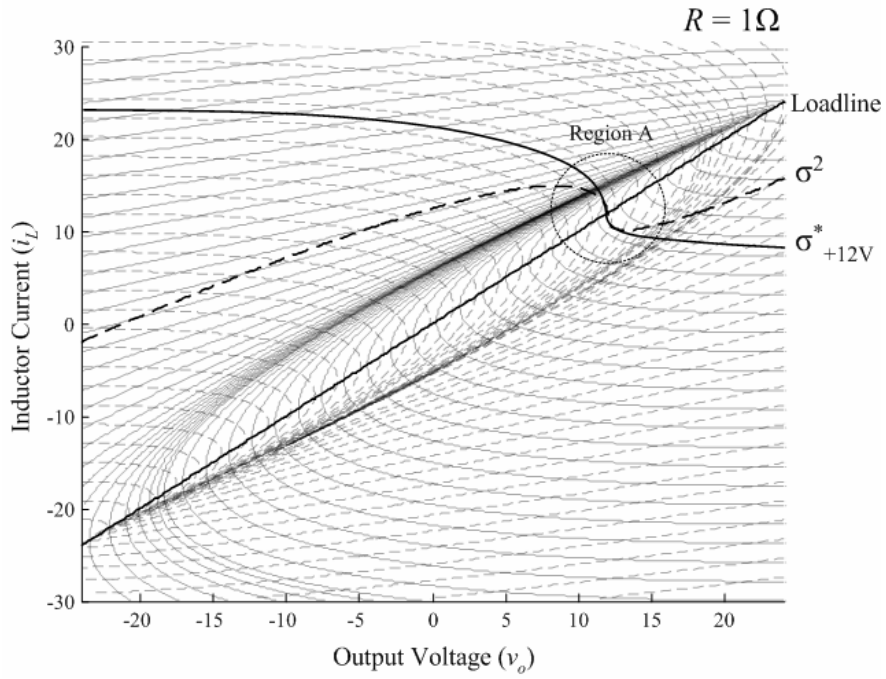
A family of the state-space trajectories and the load line are shown in Fig. 3.2. Fig. 3.2(a) shows the characteristics when $R = 5\Omega$. Fig. 3.2(b) shows the characteristics when $R = 1\Omega$. The component values used in the analysis are tabulated in Table 3.1. The trajectories consist of two main types - the *positive-state trajectories* and the *negative-state trajectories*. They are obtained by solving (3.1) with different initial conditions. The positive-state trajectory is obtained by setting $\{q_1, q_2\} = \{1, 0\}$, while the negative-state trajectory is obtained by setting $\{q_1, q_2\} = \{0, 1\}$. As discussed in [Munzert and Krein 1996], the tangential component of the state-trajectory velocity on the switching surface determines the rate at which successor points approach or recede from the target operating point. An ideal switching surface σ^* that gives optimum dynamics should be on the only trajectory passing through the target operating point. σ^* for target operating point at +12V is shown in Fig. 3.2. For dc-ac application, the output voltage v_o is time varying and follow the reference signal. Therefore, the target operating point of σ^* is also time-dependent. Although σ^* can achieve steady-state

operation for a step change in the output current or reference voltage in one on/off control, it is load-dependent and requires sophisticated computation for solving the only positive- and negative-state trajectory that passes each of the target operating points in a time varying system.

A second-order surface σ^2, which is close to the ideal surface around the operating point, is derived in the following. The concept is based on estimating the state trajectory after a hypothesized switching action. As the switching frequency of the switches is much higher than the signal frequency, the output current i_o is relatively constant over a switching cycle. The gate signals to the switches are determined by the following criteria.



(a)



(b)

Fig. 3.2 Positive- and negative-state trajectories, loadline, σ^* and σ^2 of the inverter. (a) $R = 5\ \Omega$. (b) $R = 1\ \Omega$.

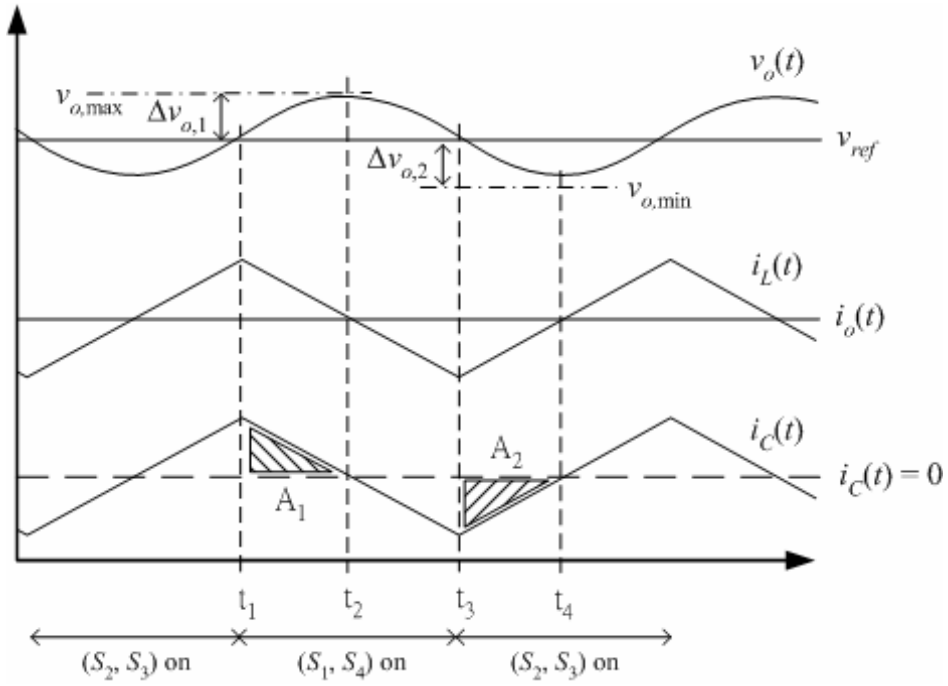


Fig. 3.3 Typical waveforms of v_o, i_L, i_o and i_C.

3.2.1 Criteria for switching on S_1 and S_4

Fig. 3.3 shows the typical waveforms of v_o, i_L, i_o and i_C. (S_1, S_4) are originally off and are switched on at the hypothesized time instant t_1, so that v_o equals $v_{o,\max}$ at t_2 (at which $i_C = 0$). Thus,

$$i_C = C\frac{dv_C}{dt} = C\frac{dv_o}{dt} \tag{3.2}$$

$$-\left(v_{in} + v_o\right) = L\frac{di_L}{dt} \tag{3.3}$$

By using $i_L = i_C + i_o$ and assuming i_o to be constant,

$$\frac{di_C}{dt} = \frac{di_L}{dt} = -\frac{v_{in} + v_o}{L} \Rightarrow dt = -\frac{L}{v_{in} + v_o}di_C \tag{3.4}$$

Based on (3.2),

$$\Delta v_{o,1} = v_o(t_2) - v_o(t_1) = v_{o,\max} - v_o(t_1) = \frac{1}{C}\int_{t_1}^{t_2} i_C dt \tag{3.5}$$

By substituting (3.4) and $i_C(t_2) = 0$ into $\frac{1}{C}\int_{t_1}^{t_2} i_C dt$, eq. (3.5) can be expressed to ensure that v_o will not go above $v_{o,\max}$, (S_1, S_4) should be switched on when

$$v_o(t_1) \geq v_{o,\max} - \frac{L}{2C\left(v_i + v_o\right)}{i_C}^2(t_1) = v_{o,\max} - k_1(v_i, v_o){i_C}^2(t_1) \tag{3.6}$$

and

$$i_C(t_1) > 0 \tag{3.7}$$

3.2.2 Criteria for switching on S_2 and S_3

As shown in Fig. 3.3, (S_2, S_3) are originally off and are switched on at the hypothesized time instant t_3, so that v_o equals $v_{o,\min}$ at t_4 (at which $i_C = 0$). Thus,

$$i_C = C\frac{dv_C}{dt} \tag{3.8}$$

$$v_{in} - v_o = L\frac{di_L}{dt} \tag{3.9}$$

By using $i_L = i_C + i_o$ and assuming i_o to be constant,

$$dt = \frac{L}{v_{in} - v_o} di_C \tag{3.10}$$

Based on (3.8),

$$\Delta v_{o,2} = v_o(t_4) - v_o(t_3) = v_{o,\min} - v_o(t_3) = \frac{1}{C}\int_{t_3}^{t_4} i_C dt \tag{3.11}$$

By substituting (3.10) and $i_C(t_4) = 0$ into $\frac{1}{C}\int_{t_3}^{t_4} i_C dt$, eq. (3.11) can be expressed to ensure that v_o will not go below $v_{o,\min}$, (S_2, S_3) should be switched on when

$$v_o(t_3) \le v_{o,\min} + \frac{L}{2C\left(v_{in} - v_o\right)} {i_C}^2(t_3) = v_{o,\min} + k_2(v_i, v_o){i_C}^2(t_3) \tag{3.12}$$

and

$$i_C(t_3) < 0 \tag{3.13}$$

Based on (3.6), (3.7), (3.12), (3.13) and $v_{o,\min} = v_{o,\max} = v_{ref}$, the following σ^2 can be concluded,

$$\sigma^2(i_L, v_C) = \begin{cases} k_1 {i_C}^2 + \left(v_C - v_{ref}\right), & i_C > 0 \\ -k_2 {i_C}^2 + \left(v_C - v_{ref}\right), & i_C < 0 \end{cases} \tag{3.14}$$

The equation can further be written into a single expression of

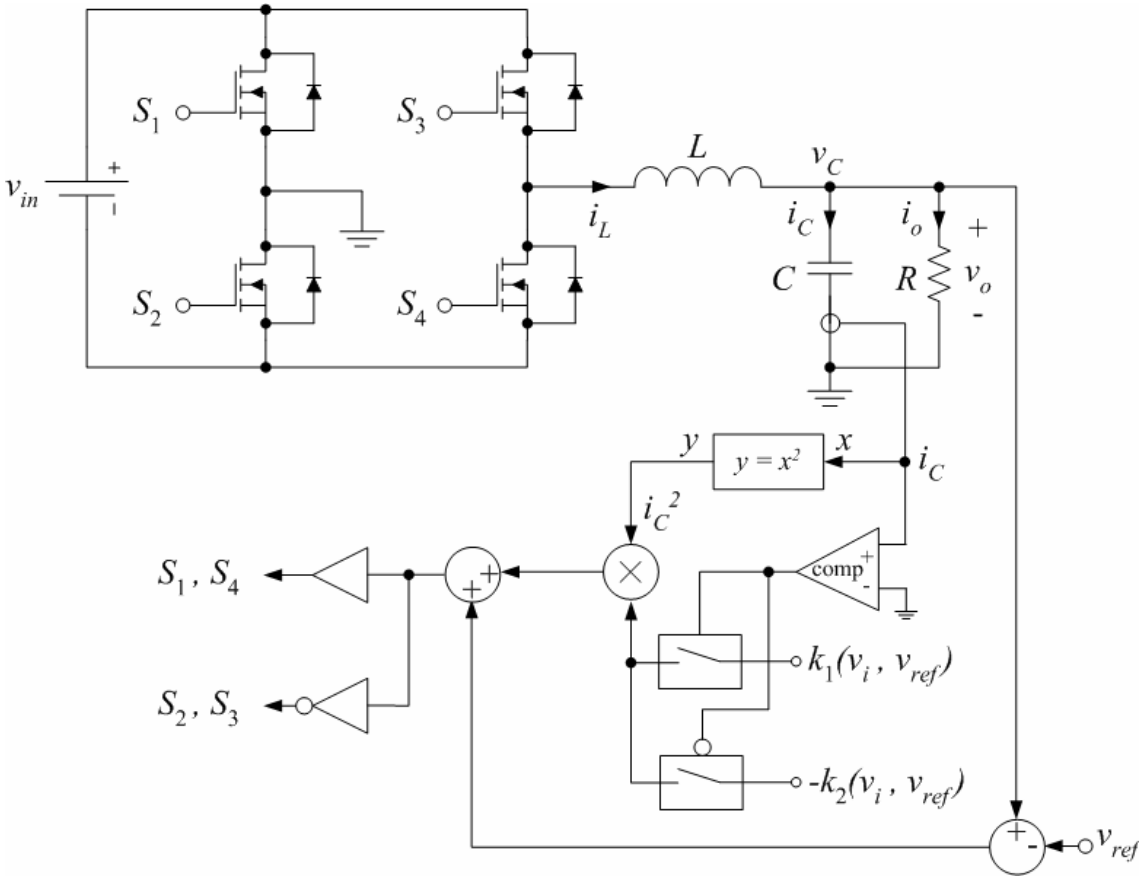
$$\sigma^2(i_L, v_C) = c_2 {i_C}^2 + \left(v_C - v_{ref}\right) \tag{3.15}$$

where $c_2 = \frac{k_1}{2}\left(1 + \mathrm{sgn}\left(i_C\right)\right) - \frac{k_2}{2}\left(1 - \mathrm{sgn}\left(i_C\right)\right)$.

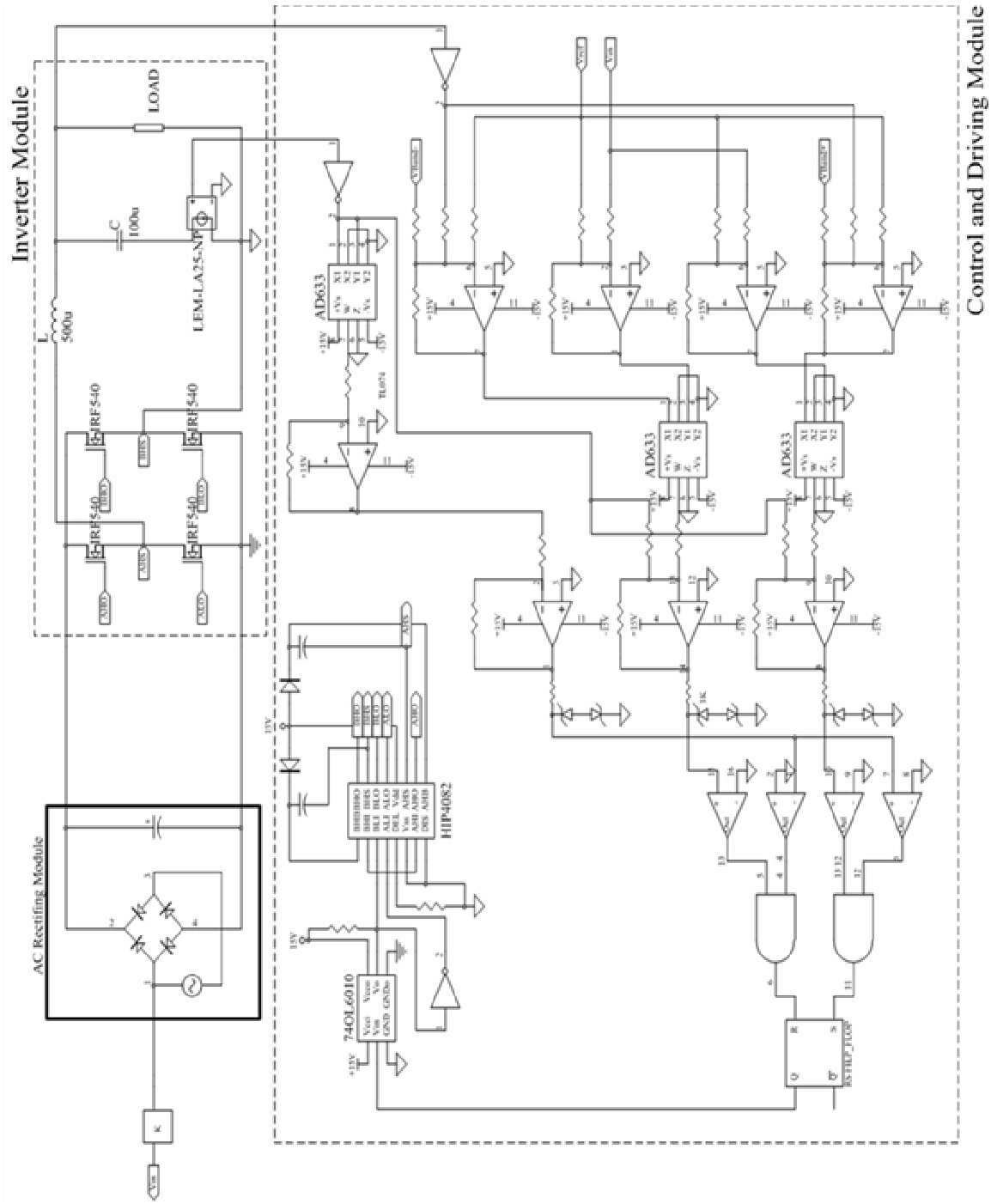
σ^2 consists of a second-order term and is close to σ^* near the operating point. However, discrepancies occur, when the state is far from the operating point because of the approximations in (3.4) and (3.10). Fig. 3.2 shows that the discrepancy increases between σ^* and σ^2 when R decreases. However, near the target operating point ("Region A"), both σ^* and σ^2 are still approximately equal. A phenomenon can be observed from Fig. 3.2(b), for any initial states below σ^2, the positive-state trajectory finally enters "Region A", where σ^2 maintains the ideal switching surface property.

However, the negative-state trajectories may not go towards "Region A", but after one switching action. Thus, it might require extra switching actions to go to the steady-state.

The control circuit can be implemented by using simple analog devices. Multipliers are required to compute the function of k_1, k_2, and i_C^2, the remaining parts can be handled by using a simple logic circuitry. Fig. 3.4(a) shows the block diagram of the controller. Fig. 3.4(b) shows the circuit schematic. The dc input stage of the inverter is connected to an ac rectifying module. Its main purpose is to test the inverter and the proposed controller output characteristics, when the input consists of undesirable harmonics. The results will be discussed in Sec. V.



(a) Block diagram.



(b) Circuit schematic.

Fig. 3.4 Implementation of the controller.

3.3 Large-Signal Stability

Points along σ = 0 can be classified into refractive, reflective, and rejective modes. The dynamics of the system will be exhibited differently in these regions. For σ^2, the transition boundary is obtained by differentiating (3.15) so that

$$\left.\frac{di_L}{dv_C}\right|_{on,off} = \frac{1}{R} + \frac{1}{2}\frac{i_L - \frac{v_C}{R}}{v_C - v_{ref}} \tag{3.16}$$

Detail derivation can be found in the section 3.7 Appendix. And the expression at the left-hand side can be derived by using the state equations in (3.1). Based on (3.16), the transition boundary with (S_2, S_3) on is

$$\frac{C}{L}\left(\frac{v_i - v_C}{i_L - \frac{v_C}{R}}\right) = \frac{1}{R} + \frac{1}{2}\frac{i_L - \frac{v_C}{R}}{v_C - v_{ref}} \tag{3.17}$$

And the transition boundary with (S_1, S_4) on is

$$-\frac{C}{L}\left(\frac{v_i + v_C}{i_L - \frac{v_C}{R}}\right) = \frac{1}{R} + \frac{1}{2}\frac{i_L - \frac{v_C}{R}}{v_C - v_{ref}} \tag{3.18}$$

Fig. 3.5 shows the transition boundaries of the inverter. σ^2 is almost along the boundary between the reflective and refractive regions, when the state is near the operating point. The state of the converter will move along the switching surface in the reflective region, which is similar to the sliding-mode control. Once the state enters into the boundary between the reflective and refractive regions, the system will go to the target operating point in the next switching action.

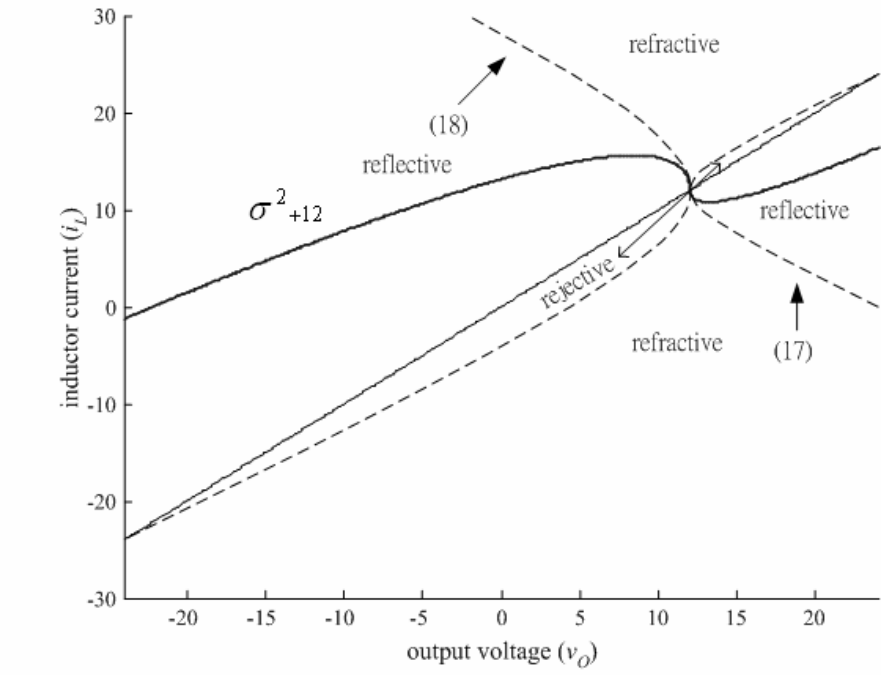
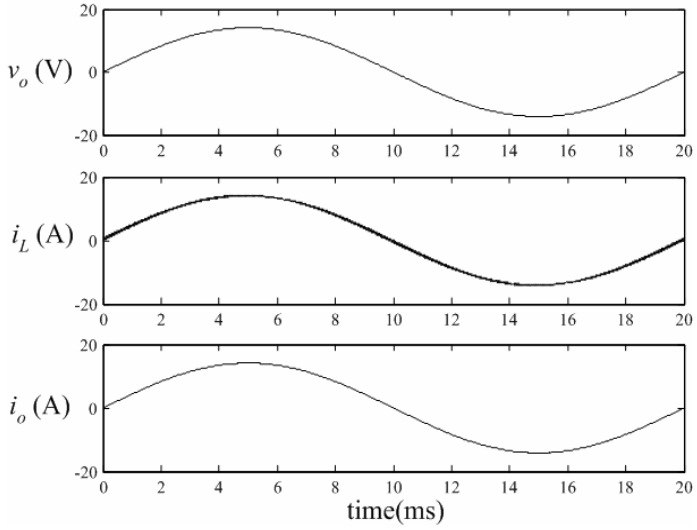


Fig. 3.5 Transition boundaries of the inverter.

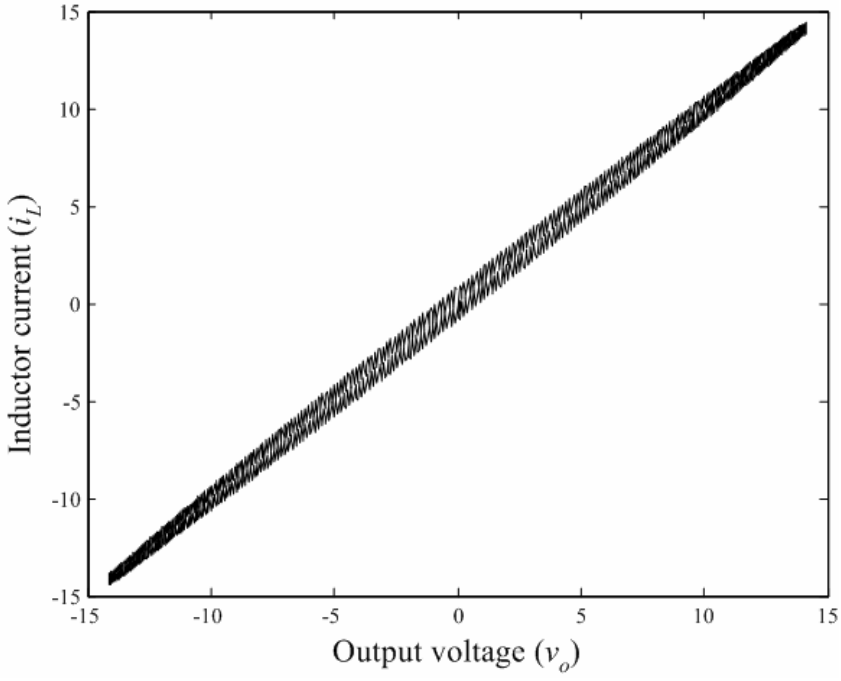
3.4 Simulation Verifications

An inverter with the component values tabulated in Table I is studied. Fig. 3.6 shows the steady-state performance of the inverter operated at R = 1 Ω and $v_{o,\text{rms}}$ = 10 V_{rms}. Fig. 3.7 shows the dynamic responses (the time-domain waveforms in Fig. 3.7(a) and the phase plane in Fig. 3.7(b)) of the inverter under a load change from 5 Ω to 1 Ω and vice versa. σ^2 determines the switching actions of the switches when the converter is subject to a large signal disturbance. In fig. 3.7(b), just before the load change from 1 Ω to 5 Ω, the output voltage is approximately equal to 14 V (i_o = 14 A). When the load change to 5 Ω, $[i_L \quad v_C]$ below σ^2 and the movement of $[i_L \quad v_C]$ will follow the positive-state trajectory until it touch the switching surface. σ^2 is nearly the same as the ideal switching surface when final states of $[i_L \quad v_C]$ is near the target operating point. Therefore, the output can revert back to the ac profile in two switching action. Figs. 3.8 and 3.9 show a comparison between σ^2 and standard PWM control with natural sampling. By comparing the simulated results, σ^2 have higher peak inductor current

during transient but give a better output profile compares with PWM control. In fact, PWM control is a linearized control which only target for small signal and steady-state performance. However, the inverter system is a nonlinear system, and σ^2 is a second order control which can be used to approximate the nonlinear trajectories nature of the inverter system in order to deal with large-signal disturbances.

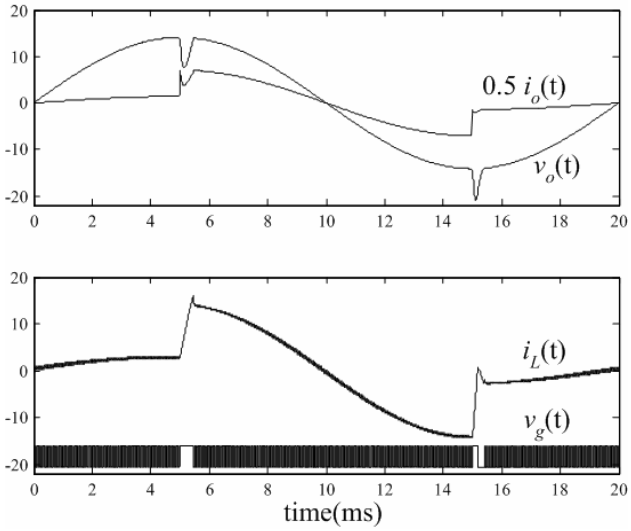


(a)

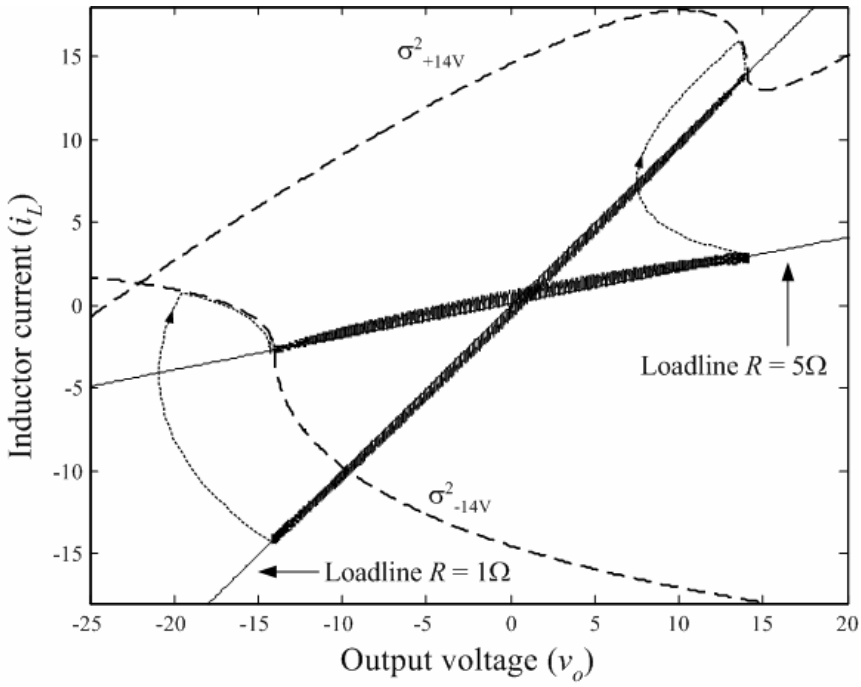


(b)

Fig. 3.6 Steady-state performance of the inverter when R = 1 Ω. (a) Time-domain. (b) State-plane.

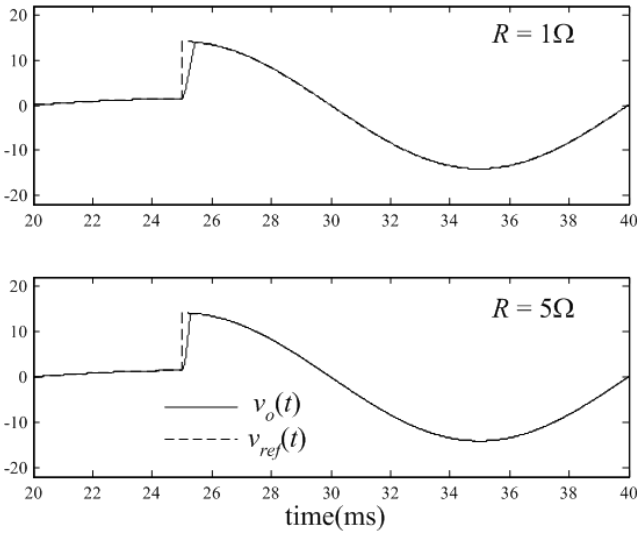


(a)

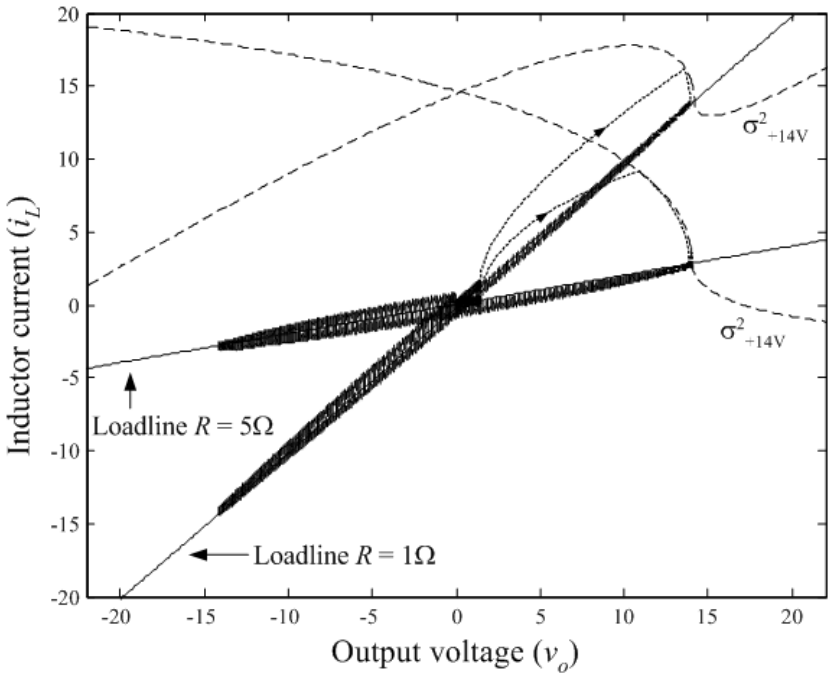


(b)

Fig. 3.7 Dynamics performances of the inverter under load change from 5 Ω to 1 Ω and vice versa. (a) Time-domain. (b) State-plane.

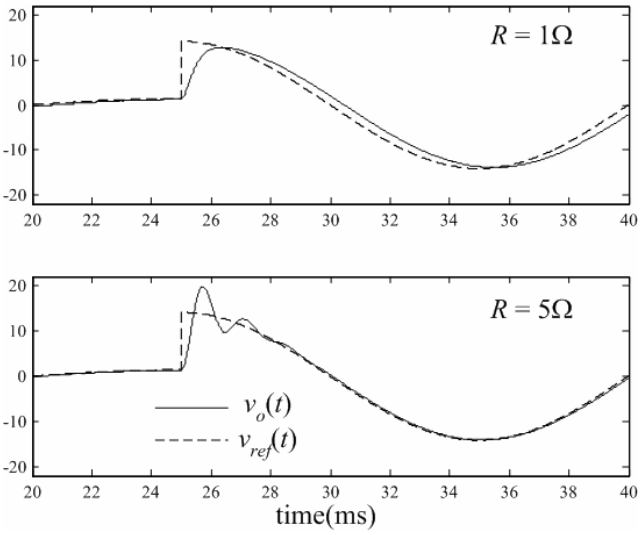


(a)

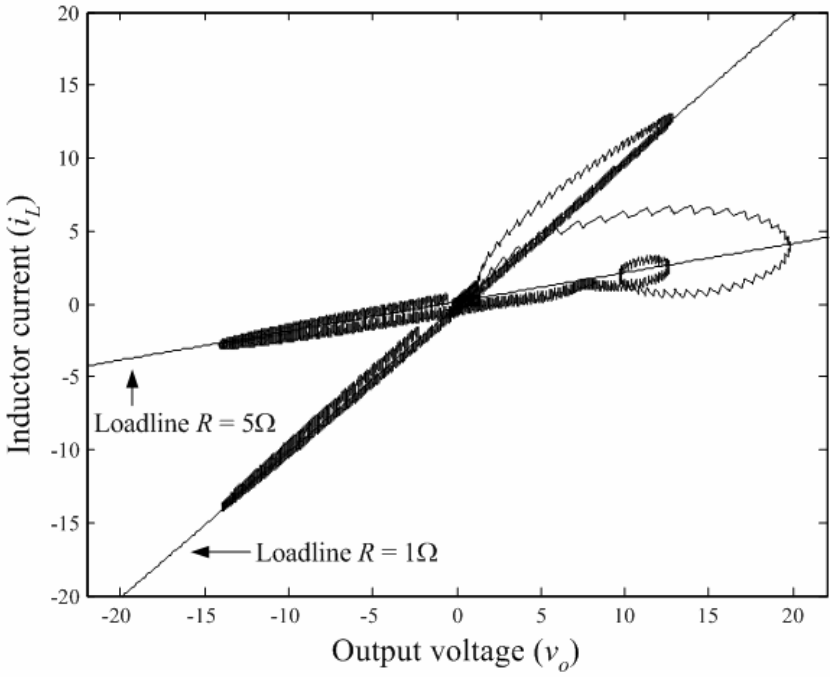


(b)

Fig. 3.8 Output voltage tracking with σ^2 for R = 1 Ω and 5 Ω. (a) Time-domain. (b) State-plane.



(a)



(b)

Fig. 3.9 Output voltage tracking with PWM for R = 1 Ω and 5 Ω.. (a) Time-domain. (b) State-plane.

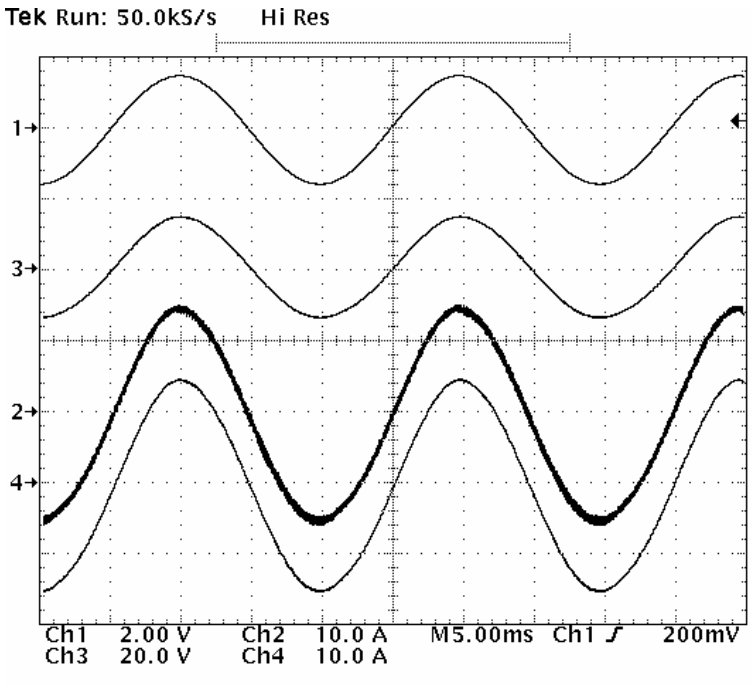
3.5 Experimental Verifications

A 100 W full bridge inverter has been built to verify the theoretical prediction and simulation results. The circuit and test setup are shown in Fig. 3.4(b). The component values of the experimental prototype are tabulated in Table 3.1. Fig. 3.10 shows the steady state operation when R = 1 Ω (full load) and R = 5 Ω. The output voltage is regulated at 10 V_{rms}. Fig. 3.11 shows the transient response when R is changed from 5 Ω to 1 Ω. The output voltage can revert to the ac reference within two switching actions. Fig. 3.12 shows the output voltage tracking performance when R = 1 Ω, a 50 Hz ac reference, dynamic change from 10 V_{rms} to 1 V_{rms} is used to demonstrate the voltage tracking ability of the controller. Again, output voltage can obtain near optimal response for increasing or decreasing of voltage reference.

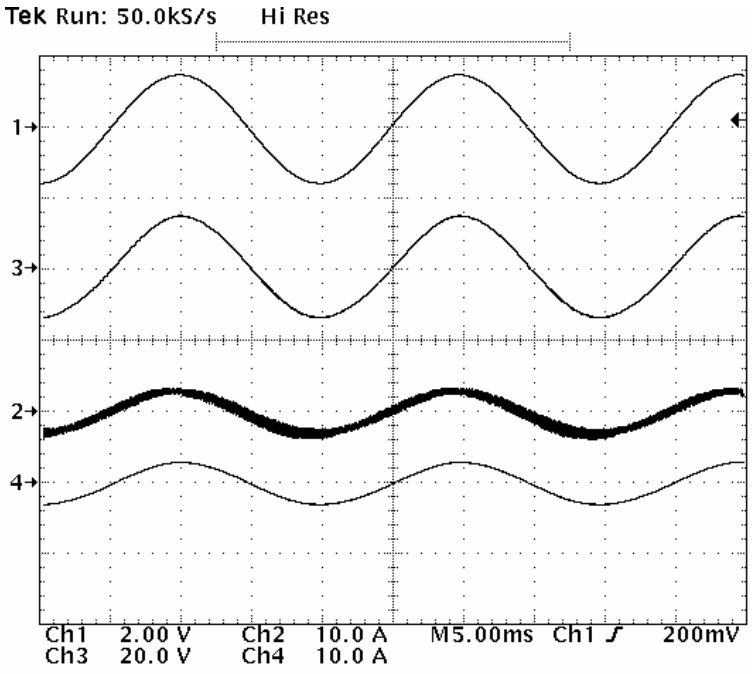
In practical application, a full-wave rectifier may be connected to the output of the full-bridge inverter for providing a rectified dc. Fig. 3.13 shows the steady-state output for a full-wave rectifier load with $i_{o,\text{rms}}$ = 2.76 A and $v_{o,\text{rectified}}$ = 9.3 V. Another practical loading condition is the inductive loading. Fig. 3.14 shows the output voltage tracking ability with inductive load. A 1 mH inductor is connected in series with a 1 Ω resistor as the load. A phase shift of 17.4^{o} (0.97ms) between v_o and i_o can be noted. Due to the load characteristics, the output voltage requires taking longer time to the steady state, as compared with the resistive load. However, the boundary control surface can still make the output follow the reference in several switching actions.

Finally, the DC input voltage source is replaced with a rectifying circuit with input capacitance equal to 2000 μF in order to shows the inverter performance with input voltage variation. Fig. 3.15 shows the response of the inverter operating at 36 W, the controller has high susceptibility to the input voltage fluctuation. As shown in the results, a 33% (8.4 $V_{p\text{-}p}$) variation in the input voltage does not affect the output waveform.

Fig. 3.16 shows the harmonic spectrum of the output voltage v_o for different loading condition. Table 3.2 lists the THD value corresponding to Fig. 3.16. The first harmonics and the noise floor are 50-60dB and 80dB, respectively, below the fundamental frequency component.

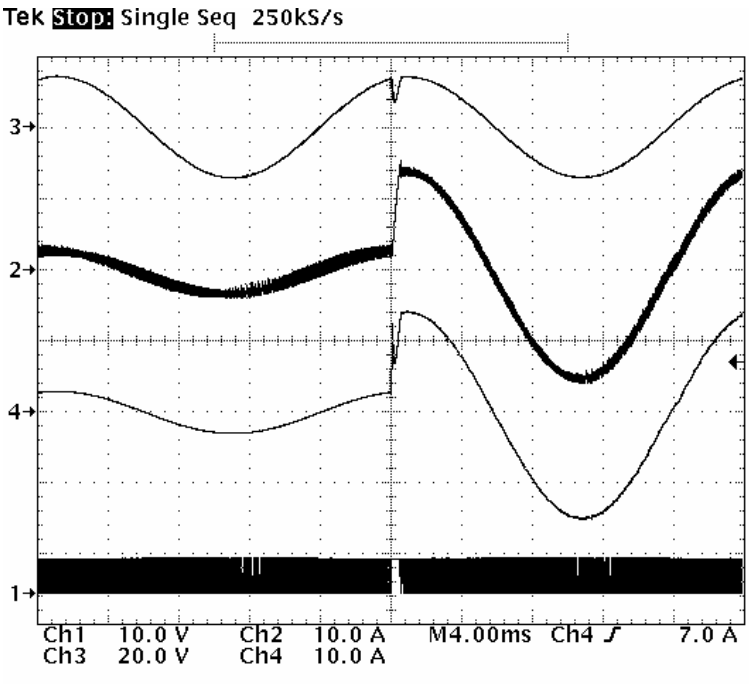


(a)

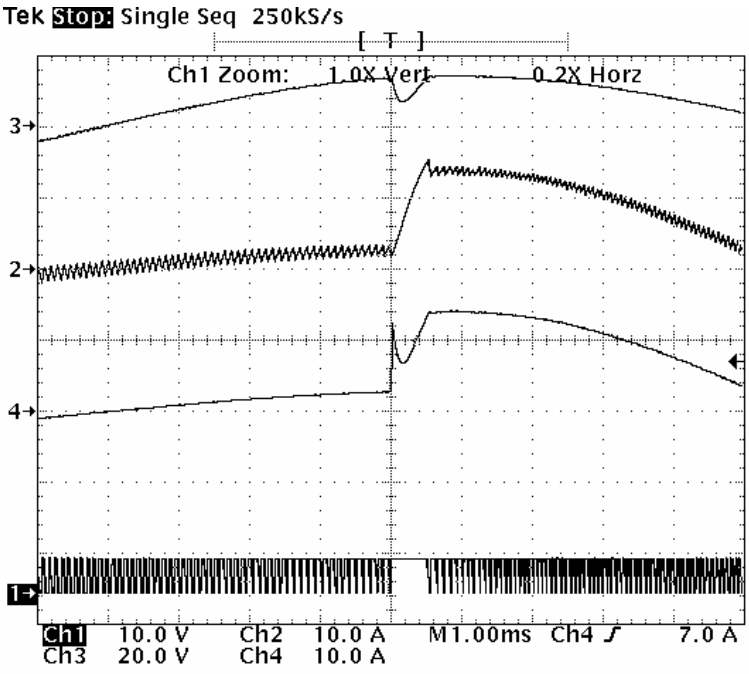


(b)

Fig. 3.10 Steady-state operation. [Ch1: v_{ref} (2V/div), Ch2: i_L(10A/div), Ch3: v_o(20V/div), Ch4: i_o(10A/div)]. (a) R = 1 Ω (full load). (b) R = 5 Ω.



(a)

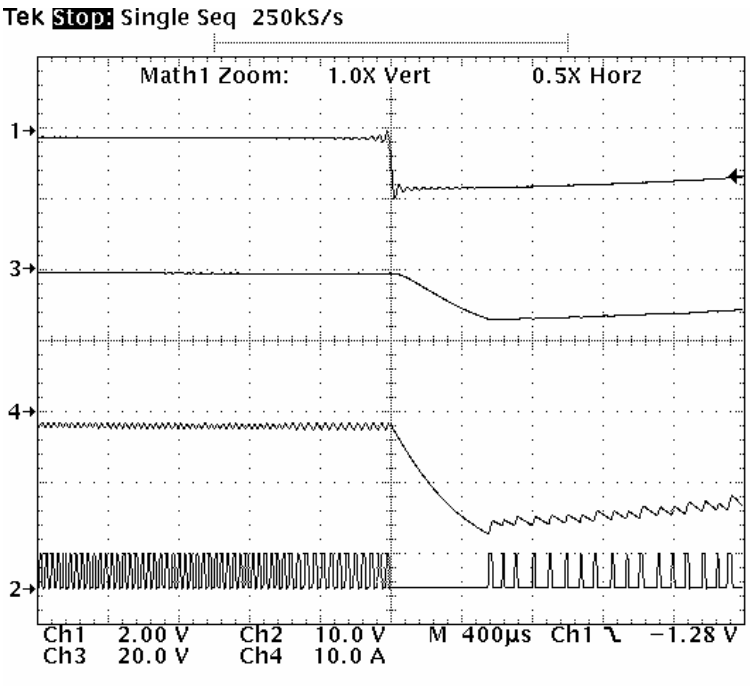


(b)

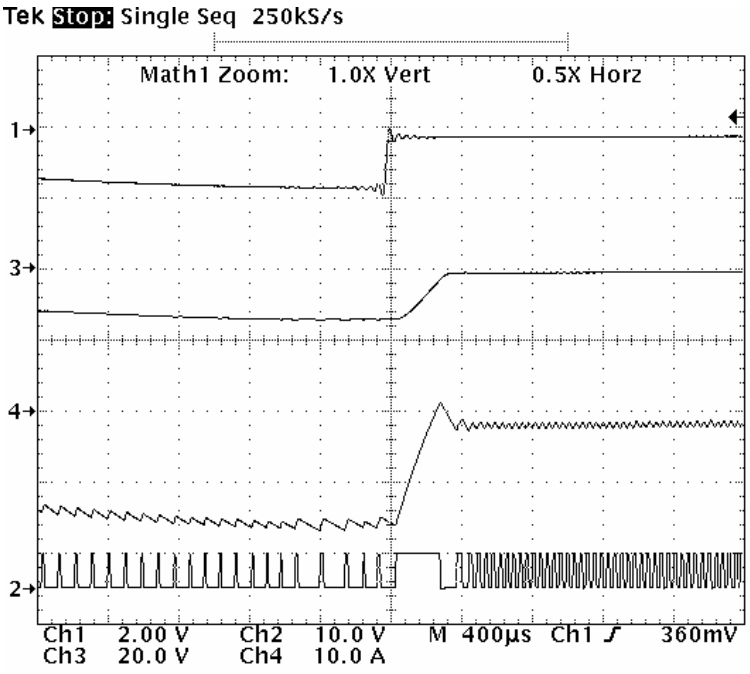
Fig. 3.11 Transient response of the full-bridge inverter when R change from 5Ω to 1Ω.

[Ch1: v_g (10 V/div), Ch2: i_L (10 A/div), Ch3: v_o (20 V/div), Ch4: i_o (10 A/div)].

(a) Timebase = 4ms. (b) Timebase = 1ms.



(a)



(b)

Fig. 3.12 Output voltage tracking when $R = 1\Omega$. [Ch1: v_{ref} (2 V/div), Ch2: v_g (10 V/div), Ch3: v_o (20 V/div), Ch4: i_L (10 A/div)]. (a) v_{ref} increases from 1 V_{rms} to 10 V_{rms}. (b) v_{ref} decreases from 10 V_{rms} to 1 V_{rms}.

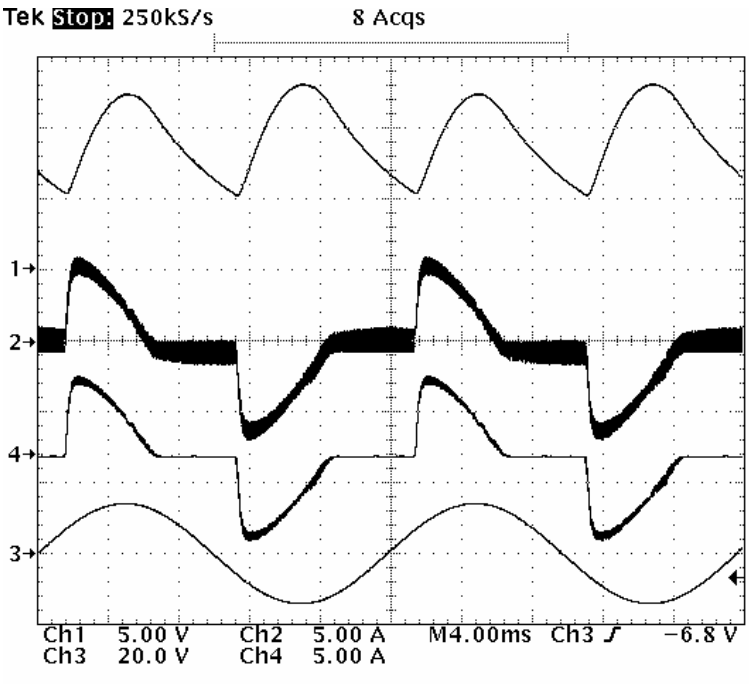
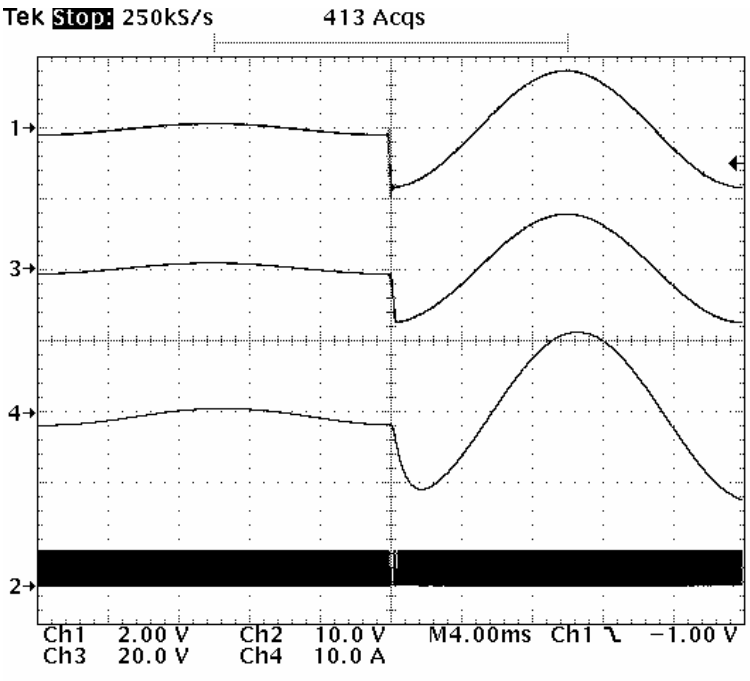
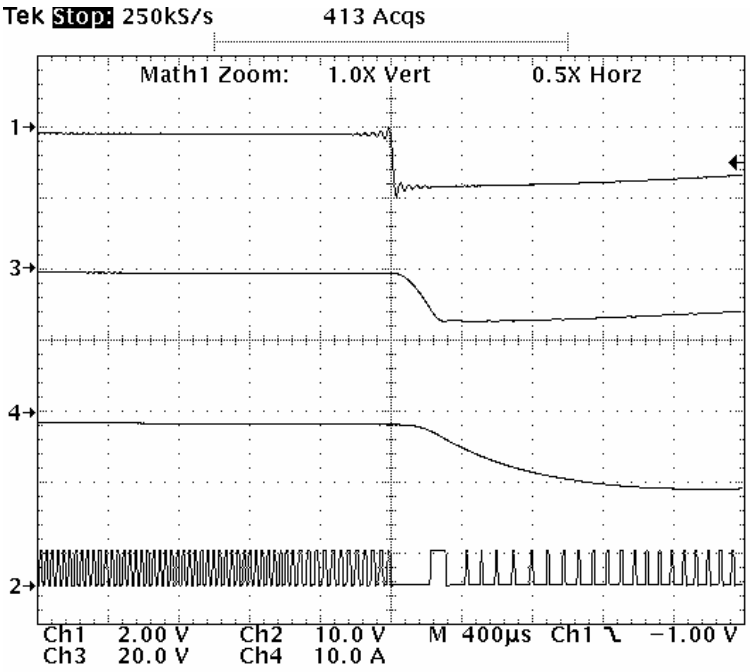


Fig. 3.13 Steady-state output for a full-wave rectifier load. [Ch1: $v_{o,\text{rectified}}$ (5 V/div), Ch2: i_L (5 A/div), Ch3: v_o (20 V/div), Ch4: i_o (5 A/div)].



(a)



(b)

Fig. 3.14 Output voltage tracking with inductive load. [Ch1: v_{ref} (2 V/div), Ch2: v_g (10 V/div), Ch3: v_o (20 V/div), Ch4: i_o (10 A/div)]. (a) Timebase = 4ms. (b) Timebase = 400us.

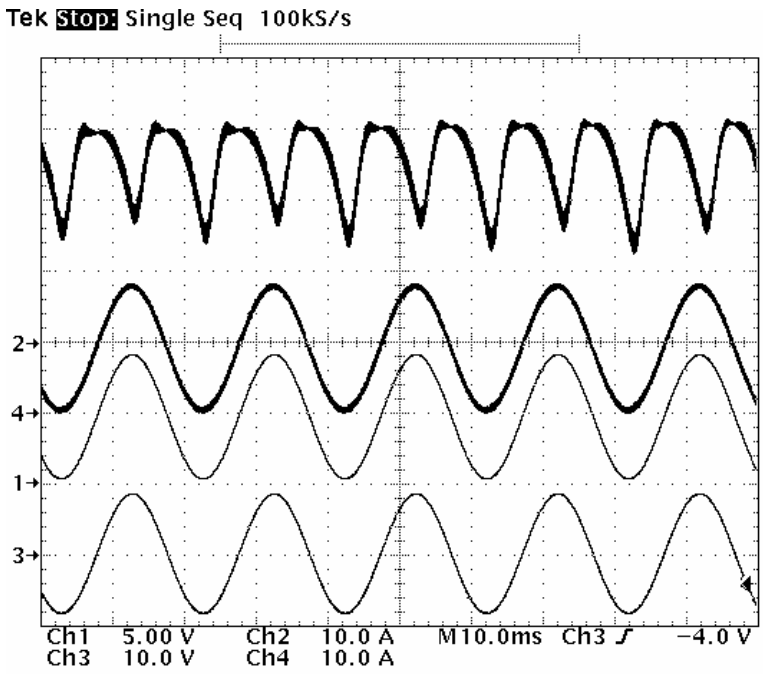
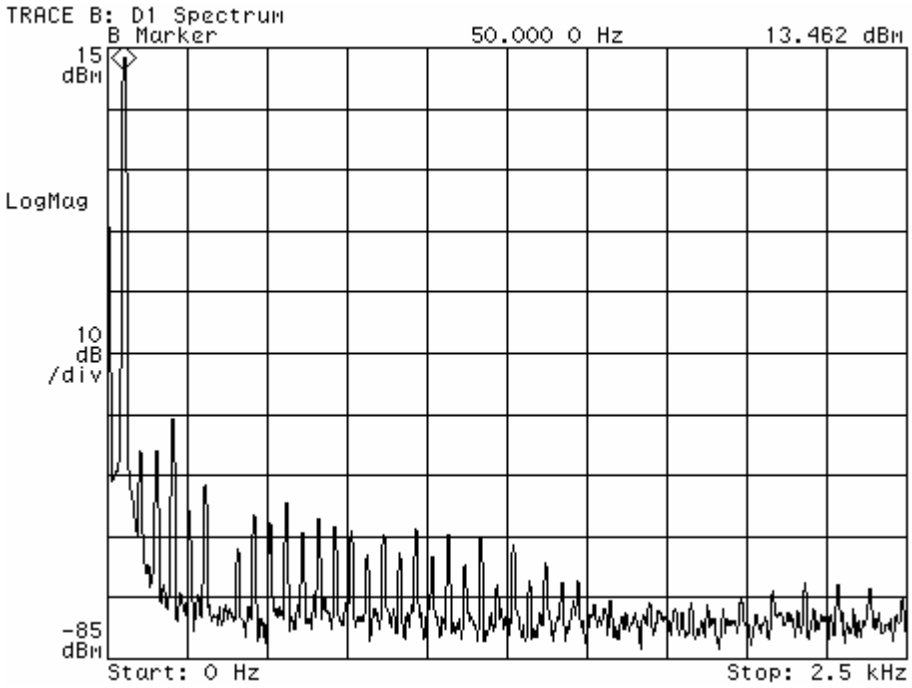
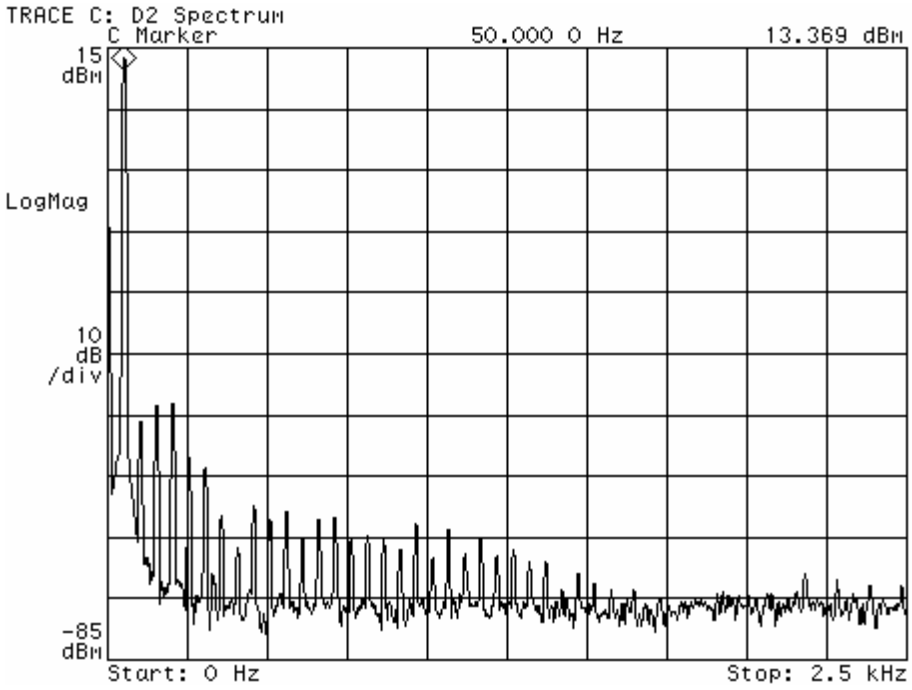


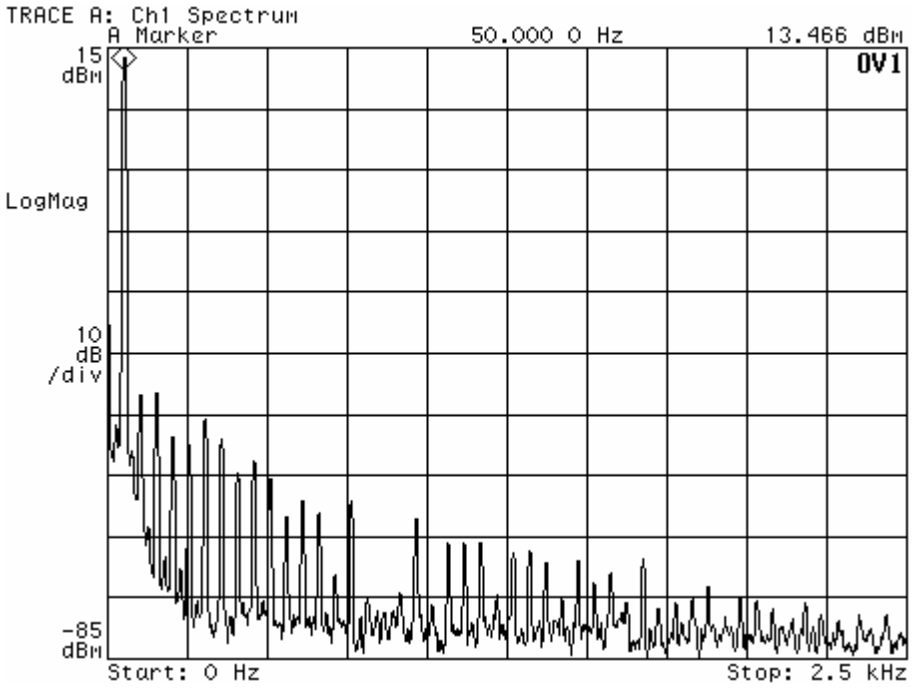
Fig. 3.15 Steady-state output with 33% of input voltage variation. [Ch1: v_i (5 V/div), Ch2: i_L (10 V/div), Ch3: v_o (10 V/div), Ch4: i_o (10 A/div)].


TRACE B: D1 Spectrum
B Marker
50.000 0 Hz
13.462 dBm
15
dBm
LogMag
10
dB
/div
-85
dBm
Start: 0 Hz
Stop: 2.5 kHz

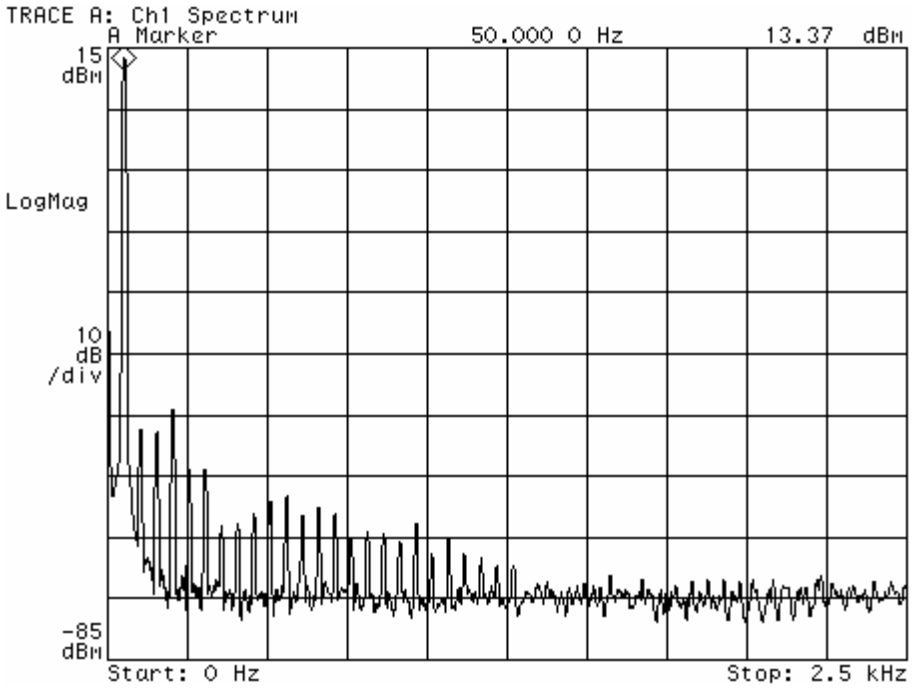
(a)


TRACE C: D2 Spectrum
C Marker
50.000 0 Hz
13.369 dBm
15
dBm
LogMag
10
dB
/div
-85
dBm
Start: 0 Hz
Stop: 2.5 kHz

(b)



(c)



(d)

Fig. 3.16 Harmonic Spectrum of the output voltage v_o with different loading condition. (a) Resistive load for $R = 5\Omega$. (b) Resistive load for $R = 1\Omega$. (c) Full wave rectified load for $P_o = 36$W. (d) Inductive load for $L = 1$ mH, $R = 1\Omega$.

Table 3.1 Component Values of the Full Bridge Inverter

Parameter	Value
v_{in}	24 V
L	500 μH
C	100 μF
R	1 Ω

Table 3.2 THD for different loading condition

v_o = 10 V_{rms} Noise Level = -80 dB Signal Freq = 50 Hz THD calculation Freq Band: dc to 2.5kHz (> 43 orders)	
Loading Condition	**THD + N%**
Resistive load with R = 5Ω	0.178046905
Resistive load with R = 1Ω	0.275200479
Full wave rectified load with P_o = 36W	0.306318266
Inductive load with L = 1 mH and R = 1Ω	0.206875159

3.6 Chapter Summary

A second-order switching surface for boundary control of DC-AC inverter is proposed in this paper. The control method is simple and does not require any complicated calculation of the system transfer function or control loop compensation. The output voltage can obtain near-optimal response when it is subject to large-signal disturbances or input voltage variation. The control methods have been studied experimentally with a 100 W inverter prototype and provide good agreement with theoretical prediction.

3.7 Appendix

3.7.1 Derivation of (3.16)

For the switching boundary (3.15), it can further be rewritten into a single expression,

$$\sigma^2 = c_2\left(i_L - \frac{v_C}{R}\right)^2 + \left(v_C - v_{ref}\right) \tag{A3.1}$$

where $c_2 = \frac{k_1}{2}\left(1+\text{sgn}\left(i_L - \frac{v_C}{R}\right)\right) - \frac{k_2}{2}\left(1-\text{sgn}\left(i_L - \frac{v_C}{R}\right)\right)$.

By differentiating both sides of (A3.1) with $\sigma^2 = 0$,

$$c_2 \frac{d\,(i_L - \frac{v_C}{R})^2}{dt} + \frac{d\,(v_C - v_{ref})}{dt} = 0$$

$$2\,c_2\,(i_L - \frac{v_C}{R})\,(\frac{d\,i_L}{dt} - \frac{1}{R}\frac{d\,v_C}{dt}) + \frac{d\,v_C}{dt} = 0$$

$$\frac{\frac{d\,i_L}{dt}}{\frac{d\,v_C}{dt}} = \frac{2\,c_2\,(i_L - \frac{v_C}{R})\frac{1}{R} - 1}{2\,c_2\,(i_L - \frac{v_C}{R})} \tag{A3.2}$$

$$\frac{d\,i_L}{d\,v_C} = \frac{1}{R} - \frac{1}{2\,c_2\,(i_L - \frac{v_C}{R})}$$

By equating $\sigma^2 = 0$ using (A3.1),

$$\frac{1}{c_2} = -\frac{(i_L - \frac{v_C}{R})^2}{v_C - v_{ref}} \tag{A3.3}$$

Substitute (A3.3) into (A3.2), it can be shown that

$$\frac{d\,i_L}{d\,v_C} = \frac{1}{R} + \frac{i_L - \frac{v_C}{R}}{2\,(v_C - v_{ref})} \tag{A3.4}$$

CHAPTER 4

USE OF THE HIGH-ORDER SWITCHING SURFACE IN THE BOUNDARY CONTROL OF INVERTERS

4.1 Introduction

This chapter presents a high-order switching surface for boundary control of inverters. In the previous chapter, σ^2 approximates the ideal switching surface (σ^*) with a second-order function, in order to achieve the objective of settling switching transients in two switching actions. Since σ^* is load-dependent and σ^2 does not have the load information, the discrepancy between σ^* and σ^2 is dependent on the damping factor of the output circuit, or equivalently the value of the load impedance (Z) with respect to the output filter natural impedance (Z_C). It will increase if Z decreases and/or the converter state is far away from the operating point. Thus, this will make the converter require more switching actions to settle to the operating point during large-signal disturbances.

This chapter gives a further enhancement on formulating the switching surface for inverters. A high-order switching surface (σ^N) is proposed. A logarithmic function is derived to approximate σ^*. The inverter exhibits better dynamic response than the ones with σ^1 or σ^2. As the load characteristics is taken into account in the switching function, σ^N is close to σ^*. The trajectory velocity along the switching surface is high that makes the trajectory ideally move toward the target operating point in two switching actions after a large-signal disturbance. The steady-state and large-signal characteristics have been studied. It will also be shown that the first-order and second-order switching surfaces are the low-order approximations of high-order switching surface. The proposed control method has been successfully applied to a 300W, 110V, 60Hz full-bridge inverter. Practical implementation of σ^N requires simple analog circuits without sophisticated digital computations. Experimental results show that the

total harmonic distortion of the output voltage is low with different load types, including resistive and nonlinear inductive loads. The system can revert to the steady state in two switching actions during large-signal disturbances in the input voltage, output load, and output reference.

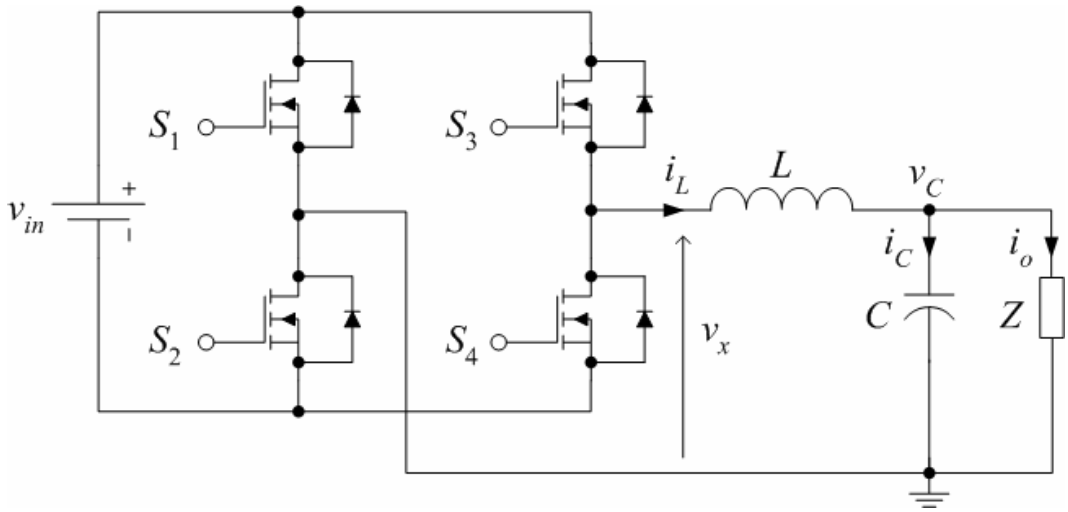


Fig. 4.1 Circuit schematic of typical full-bridge dc-ac inverter.

4.2 Principles of Operation

Fig. 4.1 shows the schematic diagram of a full-bridge inverter, which can be described by the following state-space equations

$$\dot{x} = A_0\, x + B_0\, v_{in} + (A_1\, x + B_1\, v_{in})\, q_1 + (A_2\, x + B_2\, v_{in})\, q_2 \qquad (4.1)$$

where $x = [\, i_L \;\; v_C \,]$, i_L is the inductor current, v_C is the capacitor voltage and is equal to the load voltage, v_{in} is the input voltage, q_k represents the state of the switches, and A_k and B_k are constant matrices depending on the values of L, C, and the instantaneous ac load resistance R of the load Z. (S_2, S_3) are on if $\{q_1, q_2\} = \{1, 0\}$, and (S_1, S_4) are on if $\{q_1, q_2\} = \{0, 1\}$. Matrices A_0, B_0, A_1, B_1, A_2, and B_2 are defined as

$$A_0 = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}, \quad B_0 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \quad A_1 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}, \quad A_2 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix},$$

$$B_2 = \begin{bmatrix} -1/L \\ 0 \end{bmatrix}.$$

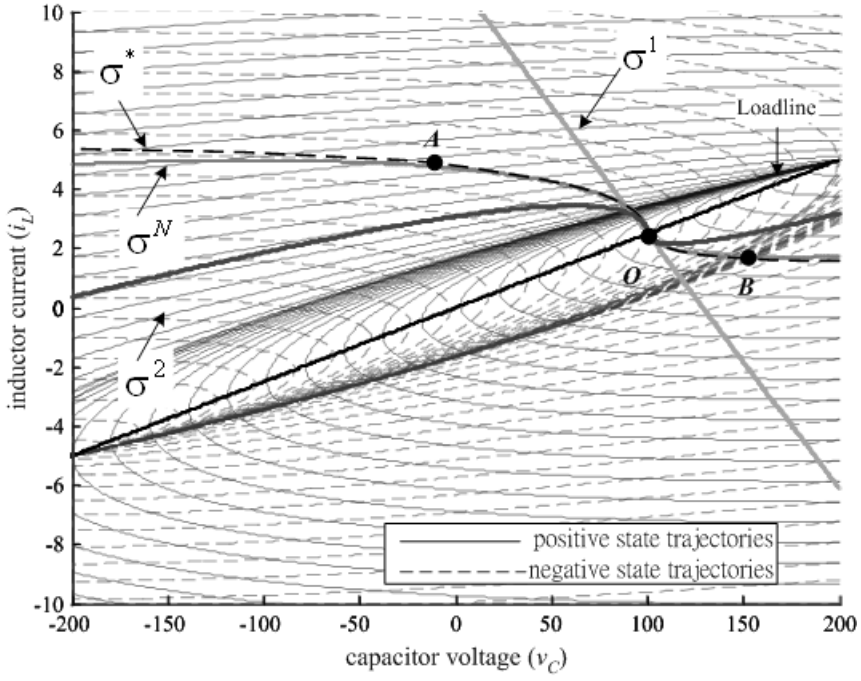


Fig. 4.2 Families of trajectories (Positive state trajectories : $v_x = v_{in}$. Negative state trajectories : $v_x = -v_{in}$).

Fig. 4.2 shows families of trajectories that are obtained by solving (1) with different initial conditions. The inverter component values used are tabulated in Table 4.1. The load is resistive and is given in Table 4.2. The *positive state trajectories* are derived, when the inverter output voltage $v_x = v_{in}$ (i.e., with S_2 and S_3 on, and S_1 and S_4 off). The *negative state trajectories* are derived, when $v_x = -v_{in}$ (i.e., with S_2 and S_3 off, and S_1 and S_4 on). The tangential component of the trajectory velocity along the switching surface determines the rate at which successor points approach or recede from the operating point 'O' [Munzert and Krein 1996]. Depending on the location of the initial state, for example the states 'A' and 'B' in Fig. 4.2, the ideal switching surface

(σ^*) is along either the only *positive state trajectory* or *negative state* trajectory that passes through 'O'. A switching surface that has deviation from σ^* will make the inverter require more switching actions to slide along the surface or to swirl around 'O' after a disturbance [Munzert and Krein 1996; Bass and Krein 1989; Greuel *et al* 1997; Leung and Chung 2005]. σ^2 has made a close approximation around the operating point [Leung and Chung 2005]. However, the settling time is still non-optimal under a large disturbance that significantly deviates from the operating point. A high-order switching surface (σ^N) that can well approximate σ^* is derived in this paper. With the help of the key waveforms shown in Fig. 4.3, the switching criteria are given as follows.

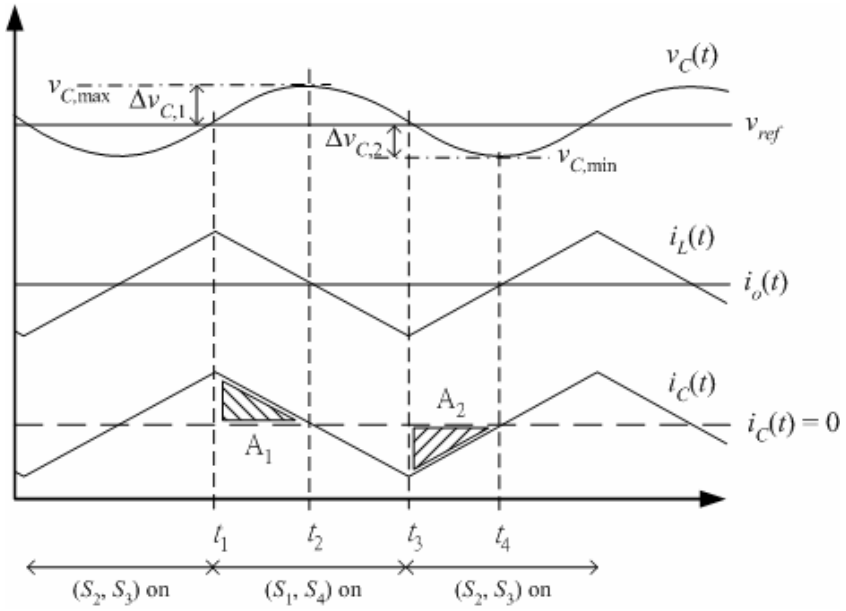


Fig. 4.3 Waveforms of v_C, i_L, i_o, and i_C.

4.2.1 Criteria for switching on S_1 and S_4

As illustrated in Fig. 4.3, S_1 and S_4 are originally off and are switched on at the hypothesized time t_1. The objective is to determine t_1, so that $v_C(t_2) = v_{C,\max}$ and $i_C(t_2) = 0$ after S_1 and S_4 are on, and the inverter will follow the negative state trajectory (Fig. 4.2). Thus, $v_C(t_1)$, $v_C(t_2)$, $i_C(t_1)$, and $i_C(t_2)$ are known values while t_2 is an

unknown value. The following assumptions have been made in deriving the switching criteria,

1) The parasitic resistances of the switches, inductor, and capacitor are neglected.

2) For the sake of simplicity in the analysis and implementation, the values of v_C and the inductor voltage v_L in the considered interval $[t_1, t_2]$ are assumed to be constant. Their values are approximated by averaging their values at t_1 and t_2. They are denoted by $\overline{V}_{C,1}$ and $\overline{V}_{L,1}$, respectively. The approximation is applicable because the switching frequency is much higher than the frequency of the reference voltage v_{ref} and the variation of v_{ref} (and thus v_C and v_L) within a switching cycle is small. Thus,

$$v_C(t) = \overline{V}_{C,1} = \frac{v_C(t_1) + v_C(t_2)}{2} = \frac{v_C(t_1) + v_{C,\max}}{2} \tag{4.2}$$

and

$$v_L(t) = \overline{V}_{L,1} = -[v_{in} + \overline{V}_{C,1})] = -\left[v_{in} + \frac{v_C(t_1) + v_{C,\max}}{2}\right] \tag{4.3}$$

for $t_1 < t < t_2$.

By applying the Kirchoff's current law at the output node,

$$\frac{di_C(t)}{dt} + \frac{v_L(t)}{L} + \frac{i_C(t)}{CR} = 0 \tag{4.4}$$

where i_o is the output current and $R = \frac{\delta v_C}{\delta i_o}$ is the instantaneous ac load resistance.

By multiplying (4.4) with $e^{\frac{t}{CR}}$ and solving it for i_C, it can be shown that

$$i_C(t) = [i_C(t_1) - k_1]\, e^{\frac{t_1 - t}{CR}} + k_1 \tag{4.5}$$

where $k_1 = \frac{C R \overline{V}_{L,1}}{L}$.

Since $i_C(t_2) = 0$,

$$t_2 = C\,R \ln\left[1 - \frac{i_C(t_1)}{k_1}\right] + t_1 \tag{4.6}$$

and $$\Delta v_{C,1} = v_C(t_2) - v_C(t_1) = v_{C,\max} - v_C(t_1) = \frac{1}{C}\int_{t_1}^{t_2} i_C(t)\,dt \tag{4.7}$$

By solving (4.7) with (4.5) and (4.6), the criteria for switching S_1 and S_4 on and S_2 and S_3 off are

$$v_C(t_1) \geq v_{C,\max} - R\left[i_C(t_1) + k_1 \ln\left(1 - \frac{i_C(t_1)}{k_1}\right)\right] \text{ and } i_C(t_1) > 0 \tag{4.8}$$

4.2.2 Criteria for switching on S_2 and S_3

As illustrated in Fig. 4.3, S_2 and S_3 are originally off and are switched on at the hypothesized time t_3. The objective is to determine t_3, so that $v_C(t_4) = v_{C,\min}$ and $i_C(t_4) = 0$ after S_2 and S_3 are on, and the inverter will follow the positive state trajectory (Fig. 4.2). Thus, $v_C(t_3)$, $v_C(t_4)$, $i_C(t_3)$, and $i_C(t_4)$ are known values while t_4 is an unknown value. Similar to Sec. A, the following assumptions have been made in deriving the switching criteria,

1) The parasitic resistances of the switches, inductor, and capacitor are neglected.

2) For the sake of simplicity in the analysis and implementation, the values of v_C and the inductor voltage v_L in the considered interval $[t_3, t_4]$ are assumed to be constant. Their values are approximated by averaging their values at t_3 and t_4. They are denoted by $\overline{V}_{C,2}$ and $\overline{V}_{L,2}$, respectively. That is,

$$\begin{aligned} v_C(t) = \overline{V}_{C,2} &= \frac{v_C(t_3) + v_C(t_4)}{2} \\ &= \frac{v_C(t_3) + v_{C,\min}}{2} \end{aligned} \tag{4.9}$$

$$v_L(t) = \overline{V}_{L,2} = v_{in} - \overline{V}_{C,2}$$

and

$$= v_{in} - \frac{v_C(t_3) + v_{C,\min}}{2} \tag{4.10}$$

for $t_3 < t < t_4$.

Again, by using (4.4) and similar technique for calculating (4.5), it can be shown that

$$i_C(t) = [i_C(t_3) - k_2]\, e^{\frac{t3-t}{CR}} + k_2 \tag{4.11}$$

where $k_2 = \dfrac{C\,R\,\overline{V}_{L,2}}{L}$.

Since $i_C(t_4) = 0$,

$$t_4 = C\,R \ln\left[1 - \frac{i_C(t_3)}{k_2}\right] + t_3 \tag{4.12}$$

and

$$\Delta v_{C,2} = v_C(t_4) - v_C(t_3) = v_{C,\min} - v_C(t_3) = \frac{1}{C}\int_{t_3}^{t_4} i_C(t)\, dt \tag{4.13}$$

By solving (4.13) with (4.11) and (4.12), the criteria for switching S_2 and S_3 on, and S_1 and S_4 off are

$$v_C(t_3) \le v_{C,\min} - R\left[i_C(t_3) + k_2 \ln\left(1 - \frac{i_C(t_3)}{k_2}\right)\right] \text{ and } i_C(t_3) < 0 \tag{4.14}$$

Fig. 4.3 shows the waveforms of the inverter with hysteresis bands added, in order to avoid frequency chattering. However, for the sake of simplicity in design and analysis, the hysteresis band is ignored in the calculations. Thus, by combining (4.8) and (4.14) and putting $v_{C,\min} = v_{C,\max} = v_{ref}$, the following switching surface σ^N is defined

$$\sigma^N(i_L, v_C) = \begin{cases} R\left[i_C + k_1 \ln\left(1 - \dfrac{i_C}{k_1}\right)\right] + (v_C - v_{ref}) \\ R\left[i_C + k_2 \ln\left(1 - \dfrac{i_C}{k_2}\right)\right] + (v_C - v_{ref}) \end{cases} \tag{4.15}$$

where $i_C = i_L - \dfrac{v_C}{R}$.

The equation can be written into a general form of

$$\sigma^N(i_L, v_C) = R\left[i_C + c_1 \ln\left(1 - \frac{i_C}{c_1}\right)\right] + (v_C - v_{ref}) \tag{4.16}$$

where $c_1 = \frac{k_1}{2}[1 + \text{sgn}(i_C)] + \frac{k_2}{2}[1 - \text{sgn}(i_C)]$ and $i_C = i_L - \frac{v_C}{R}$.

Fig. 4.2 shows σ^N in the state plane. Fig. 4.4 shows the block diagram of the proposed high-order boundary controller.

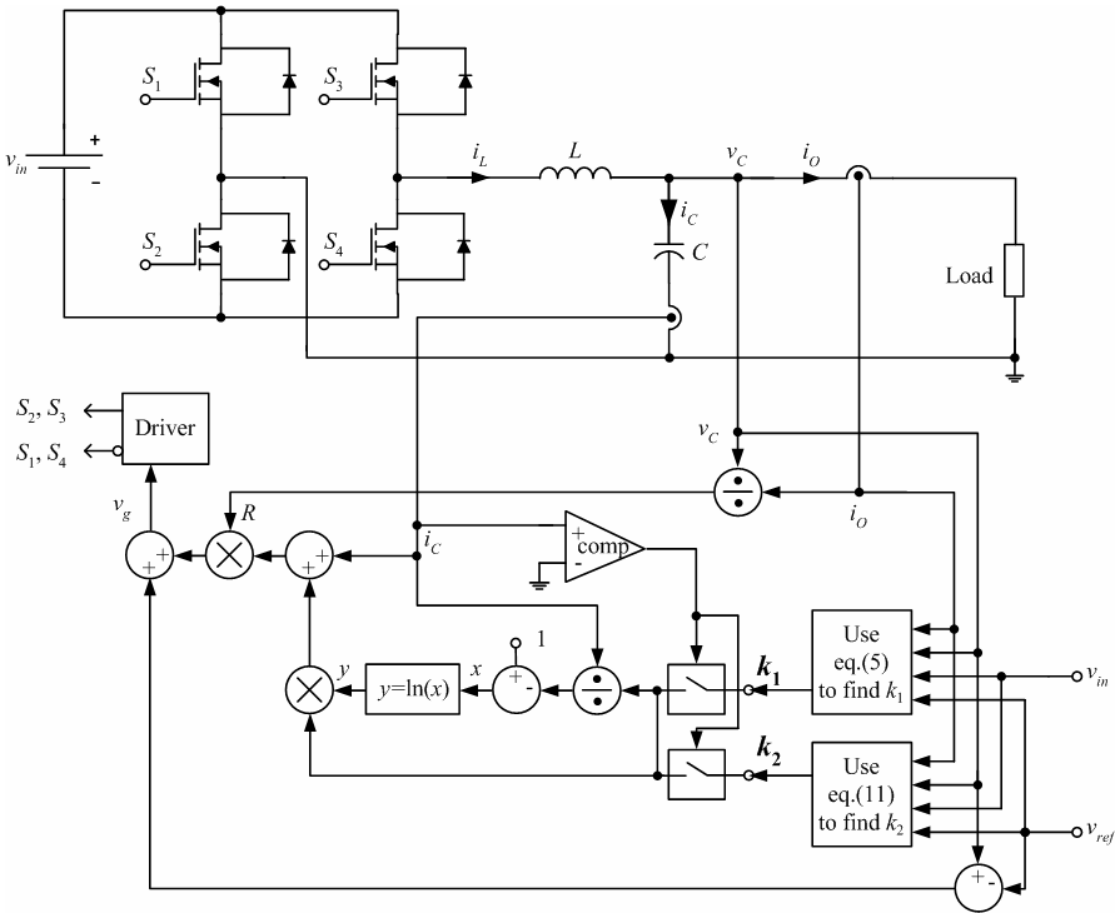


Fig. 4.4 Block diagram of the proposed high-order boundary controller.

4.3 Comparisons among σ*, σ[1], σ[2], and σ[N]

By expanding the logarithmic function in (4.16) with the Taylor series,

$$\sigma^N\,|_{N\to\infty} = R\left[i_C + c_1\left[\sum_{n=1}^{N} -\frac{1}{n}\left(\frac{i_C}{c_1}\right)^n\right]\right] + (v_C - v_{ref}) \tag{4.17}$$

and putting $N = 0, 1, 2$ respectively, it can be shown that

$$\sigma^N |_{N=0} = R\, i_C + (v_C - v_{ref}) \tag{4.18}$$

$$\sigma^N |_{N=1} = v_C - v_{ref} \tag{4.19}$$

$$\sigma^N |_{N=2} = -\frac{R}{2}\frac{i_C^{\,2}}{c_1} + (v_C - v_{ref}) \tag{4.20}$$

Eq. (4.18) gives the typical mathematical expression of the switching surface for the sliding-mode control. Eq. (4.19) gives the typical expression switching surface for the hysteresis control. By substituting the values of k_1 in (4.5) and k_2 in (4.11) for c_1 in (4.20), it can be shown that

$$\sigma^N |_{N=2} = \frac{L\, i_C^{\,2}}{2\, C\, (v_{in} + \frac{v_C + v_{ref}}{2})} + (v_C - v_{ref}) \tag{4.21}$$

for switching S_1 and S_4 on and S_2 and S_3 off, and

$$\sigma^N |_{N=2} = -\frac{L\, i_C^{\,2}}{2\, C\, (v_{in} - \frac{v_C + v_{ref}}{2})} + (v_C - v_{ref}) \tag{4.22}$$

for switching S_2 and S_3 on and S_1 and S_4 off.

Eqs. (4.21) and (4.22) give similar expressions as the switching surface σ^2 proposed in [Leung and Chung 2004; Leung and Chung 2005]. Thus, σ^2 is also the low-order approximation of σ^N.

In the following analysis, a pure mathematical treatment on comparing the discrepancies of σ^1, σ^2, and σ^N with σ^* is conducted. All switching surfaces are considered as continuous mathematical functions. No intracycle switching behaviors are taken into account. For the sake of comparison the values of v_C and i_C along the respective switching surface are normalized by the values at the operating point. The switching surfaces are compared by studying those surfaces on a $\hat{i}_C$ - $\hat{v}_C$ plane, where $\hat{i}_C$ and $\hat{v}_C$ are the normalized values of i_C and v_C, respectively.

v_C is normalized by the base value of v_{ref}. That is,

$$\hat{v}_C = \frac{v_C}{v_{ref}} \tag{4.23}$$

i_C is normalized by the base value of $i_{C,n}$, which is equal to

$$i_{C,n} = \frac{v_{ref}}{Z_C} \tag{4.24}$$

where $Z_C = \frac{1}{2}\sqrt{\frac{L}{C}}$ is the load impedance that the output filter is in critical damping. Detailed derivation of Z_C is given in Appendix.

Thus,

$$\hat{i}_C = \frac{i_C}{i_{C,n}} \tag{4.25}$$

By putting (4.23) and (4.25) into (4.16), (4.18), and (4.20), the normalized switching surfaces $\hat{\sigma}^N$, $\hat{\sigma}^1$, and $\hat{\sigma}^2$ of σ^N, σ^1, and σ^2, respectively, with different load resistances are equal to

$$\hat{\sigma}^1 = R\hat{i}_C + Z_C\hat{v}_C - Z_C \tag{4.26}$$

$$\hat{\sigma}^2 = c_1\hat{i}_C^{\,2} + \frac{Z_C^{\,2}}{v_{ref}}\hat{v}_C - \frac{Z_C^{\,2}}{v_{ref}} \tag{4.27}$$

$$\hat{\sigma}^N = R\left[\hat{i}_C + c_1\frac{Z_C}{v_{ref}}\ln\left(1 - \frac{v_{ref}}{Z_C}\frac{\hat{i}_C}{c_1}\right)\right] + (Z_C\hat{v}_C - Z_C) \tag{4.28}$$

When the inverter reaches the steady state, $v_C = v_{ref}$ and $i_C = 0$. Thus, the normalized operating point ($\hat{v}_{C,o}$, $\hat{i}_{C,o}$) on the $\hat{i}_C$ - $\hat{v}_C$ plane is

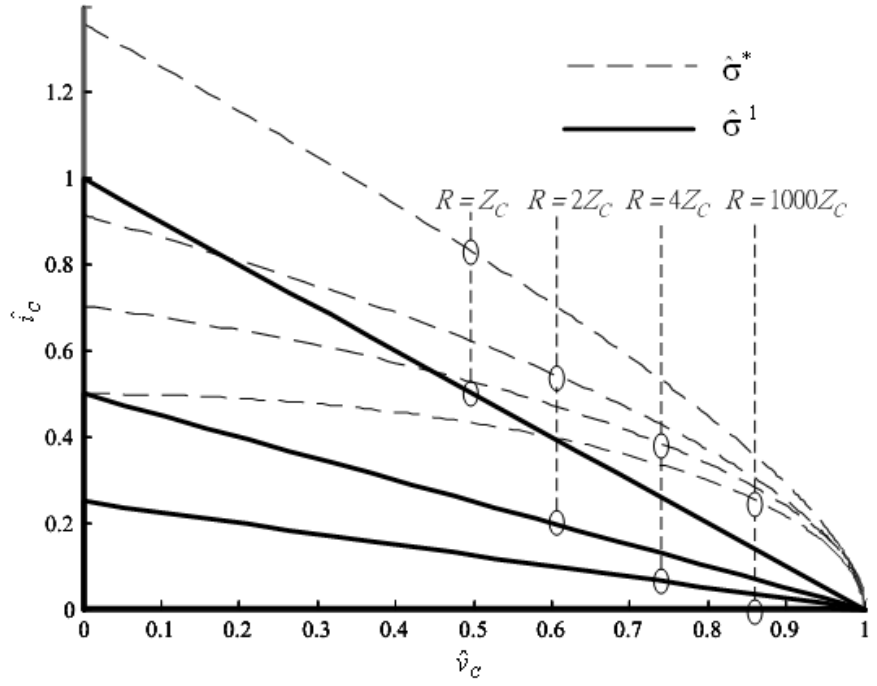
$$\hat{v}_C = 1 \tag{4.29}$$

and

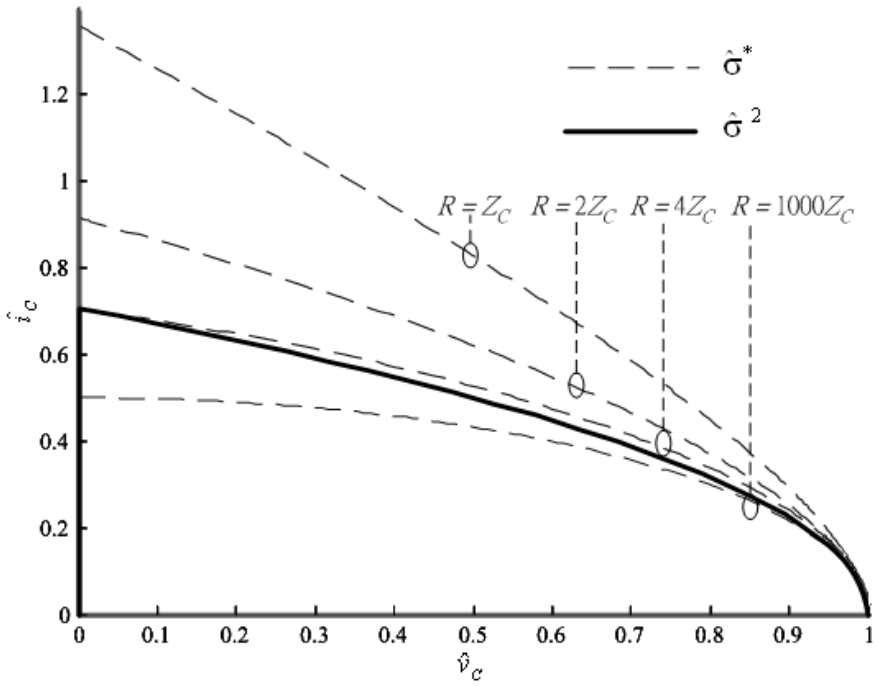
$$\hat{i}_C = 0 \tag{4.30}$$

The normalized ideal switching surface $\hat{\sigma}^*$ is obtained by putting (4.23) and (4.25) into (4.1). A comparison of $\hat{\sigma}^1$, $\hat{\sigma}^2$, $\hat{\sigma}^N$, and $\hat{\sigma}^*$ is shown in Fig. 4.5. Among

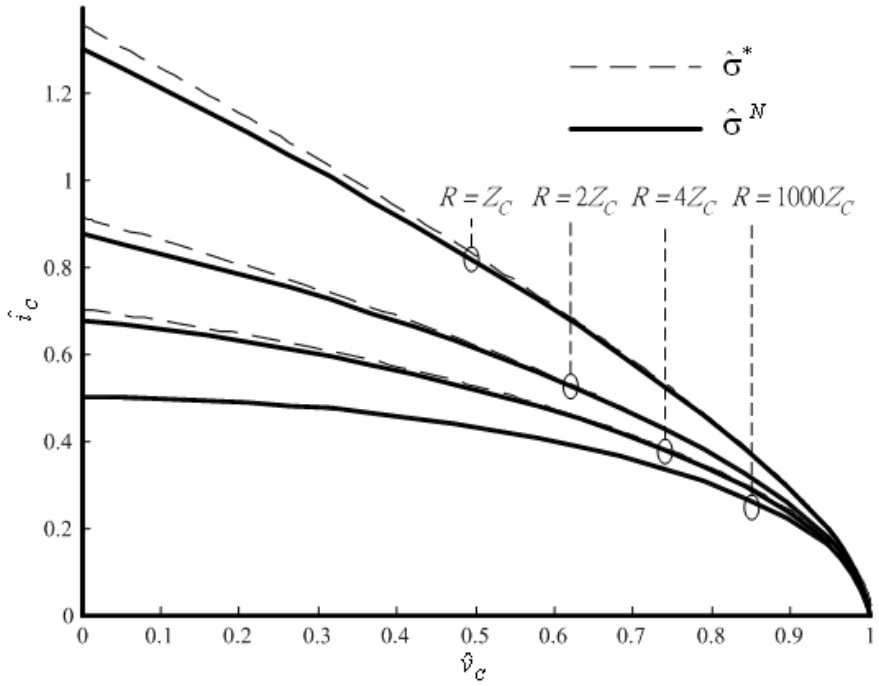
them, $\hat{\sigma}^1$ deviates considerably from $\hat{\sigma}^*$, $\hat{\sigma}^2$ gives closer approximation to $\hat{\sigma}^*$ around the operating point, and $\hat{\sigma}^N$ gives the best approximation of $\hat{\sigma}^*$ over the operating range.



(a) $\hat{\sigma}^1$.



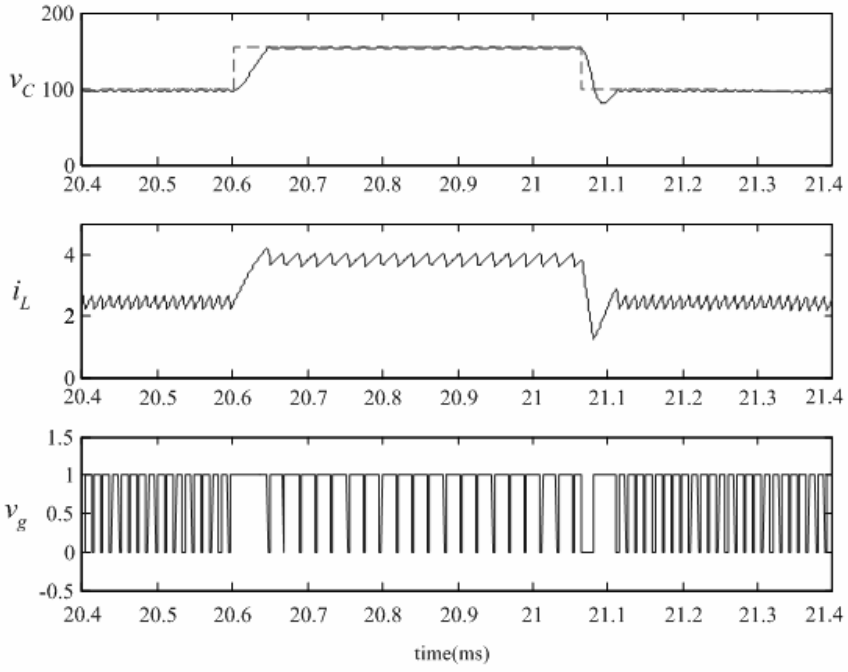
(b) $\hat{\sigma}^2$.



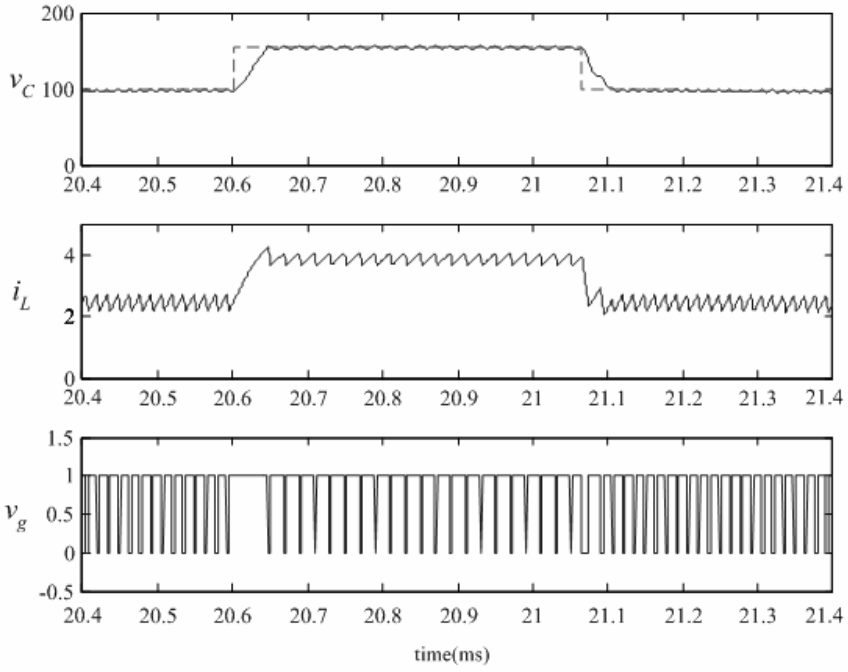
(c) $\hat{\sigma}^N$.

Fig. 4.5 Comparison of various normalized switching surfaces.

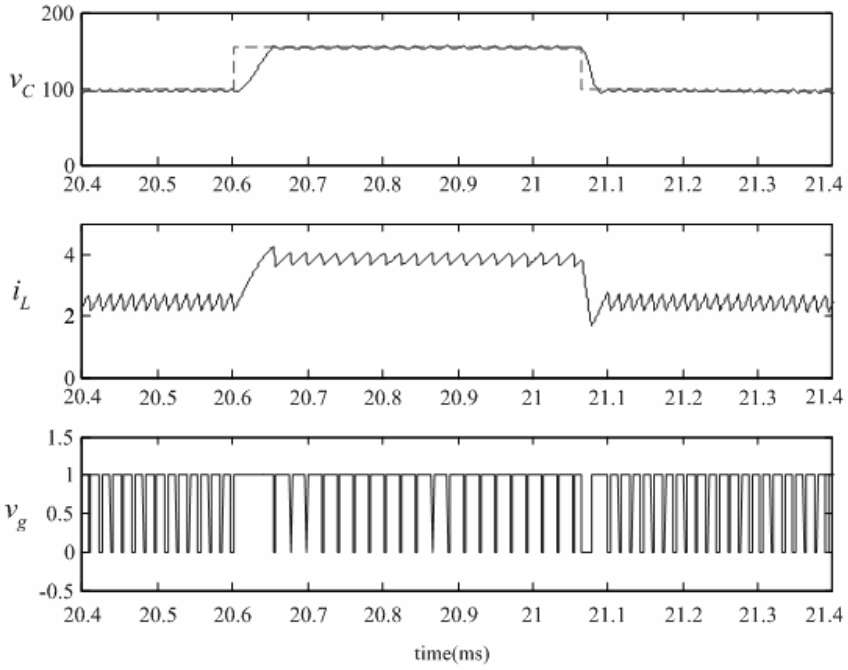
Figs. 4.6 and 4.7 show the comparisons of the simulated time-domain waveforms, including v_C, i_L, and the gate signal to S_2 and S_3, v_g, and the state-space trajectories with various switching surfaces under a large-signal reference voltage change from the peak voltage of $70V_{rms}$ (i.e., 99V) to $110V_{rms}$ (i.e., 155V) and vice versa. The parameters used are given in Table 4.1. The settling times of the system with different switching surfaces are given in Table 4.3. It can be observed that the one with σ^N gives the shortest settling time, confirming the advantages of the proposed control.



(a) σ^1.

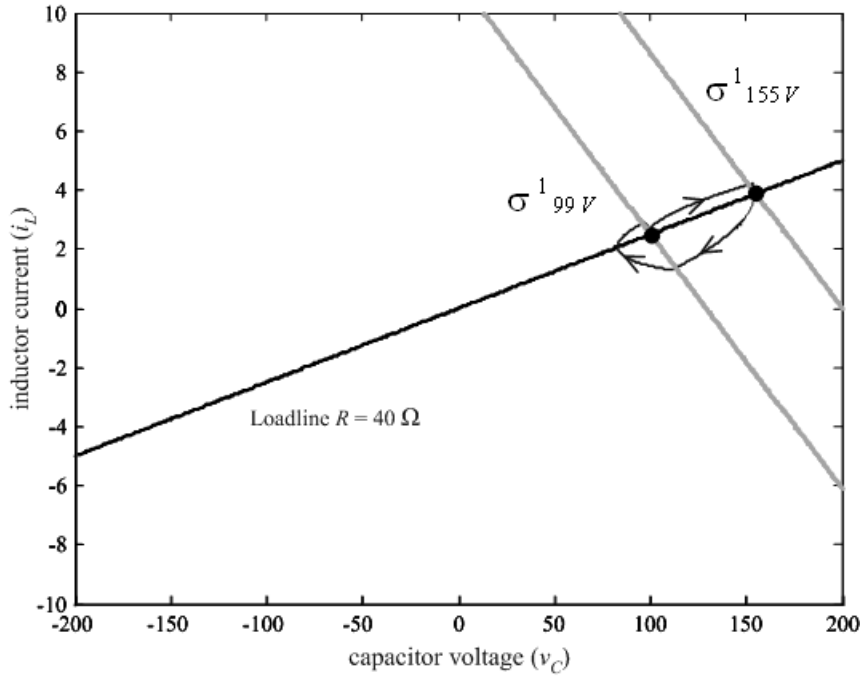


(b) σ^2.

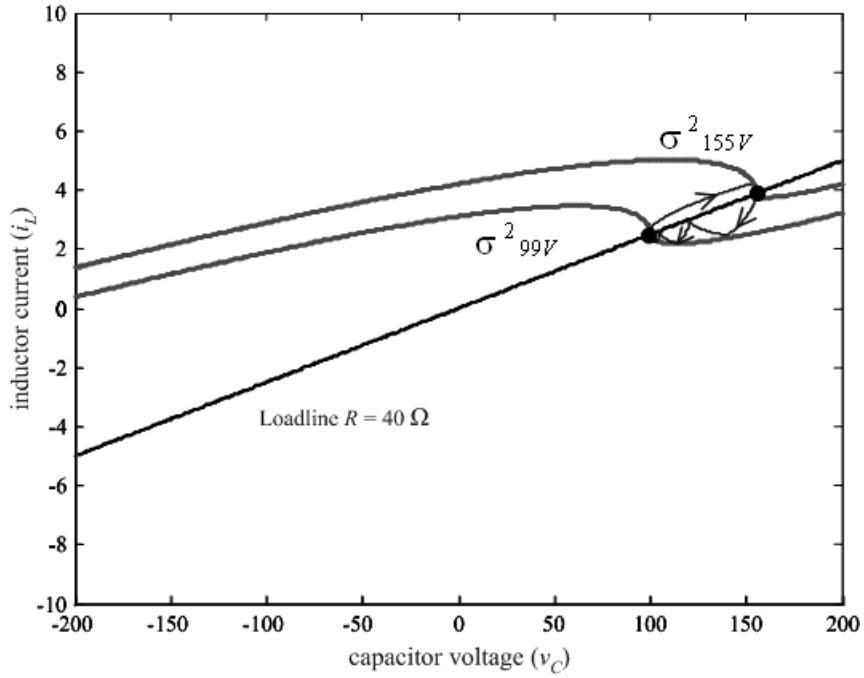


(c) σ^N.

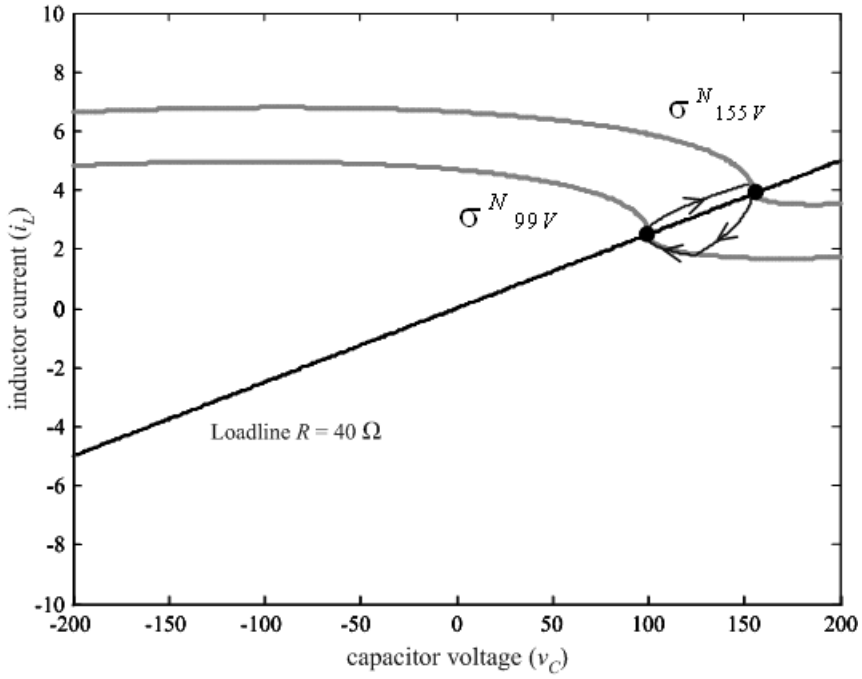
Fig. 4.6 Simulated time-domain waveforms of the inverter various switching surfaces under large-signal reference changes.



(a) σ^1.



(b) σ^2.



(c) σ^N.

Fig. 4.7 Simulated state-space trajectories of the inverter various switching surfaces under large-signal reference changes

4.4 Steady-State Characteristics

As described in Sec. III, σ^2 is the low-order approximation of σ^N. The inverter gives similar steady-state characteristics around the operating point with the two switching surfaces. Thus, in order to simplify the analysis, the steady-state characteristics of the inverter with σ^N, including the average output voltage v_{avg}, output ripple voltage v_{ripple}, and switching frequency f_s, are studied by applying the formulas in [Leung and Chung 2005] for σ^2. Based on the equations derived in [Leung and Chung 2005], v_{avg}, v_{ripple}, and f_s can be expressed as

$$v_{avg} = v_{ref} + \frac{\dfrac{L}{2C(v_{in}+v_{ref})} - \dfrac{L}{2C(v_{in}-v_{ref})} - (\beta_1 - \beta_2)}{\beta_1 + \beta_2}\Delta_N = v_{ref} \qquad (4.31)$$

$$v_{ripple} = \frac{2\,Lv_{in}\,\Delta_N}{C\,(\beta_1+\beta_2)(v_{in}+v_{ref})(v_{in}-v_{ref})} \qquad (4.32)$$

$$f_s = \frac{(v_{in} + v_{ref})(v_{in} - v_{ref})}{2\,L\,v_{in}\left(\sqrt{\frac{\Delta_N}{\beta_1}} + \sqrt{\frac{\Delta_N}{\beta_2}}\right)} \tag{4.33}$$

where $\beta_1 = \frac{L}{2\,C\,(v_{in} + v_{ref})}$, $\beta_2 = \frac{L}{2\,C\,(v_{in} - v_{ref})}$, and Δ_N is the hysteresis band.

Based on (4.31), the average output voltage is the same as the reference voltage.

Equation (4.33) can also be rewritten as,

$$f_s = \frac{1}{\alpha}\,d\,(1-d) \tag{4.34}$$

where $d = \frac{1}{2}(1 + \frac{v_{ref}}{v_{in}})$ and $\alpha = \frac{L}{2\,v_{in}}\left(\sqrt{\frac{\Delta_N}{\beta_1}} + \sqrt{\frac{\Delta_N}{\beta_2}}\right)$.

By differentiating (4.34) with respect to v_{ref}, it can be shown that

$$\frac{d\,f_s}{d\,v_{ref}} = \frac{1}{\alpha}(1 - 2\,d) \tag{4.35}$$

Thus, f_s is maximum, when d = 0.5 and v_{ref} = 0. Fig. 4.8 shows the relationships between f_s and v_{ref} (and d). They are in a parabolic function. The relationships between f_s and v_{ref} are illustrated with five operating points marked with '1' to '5'. It should be noted that f_s is much higher than the inverter output frequency.

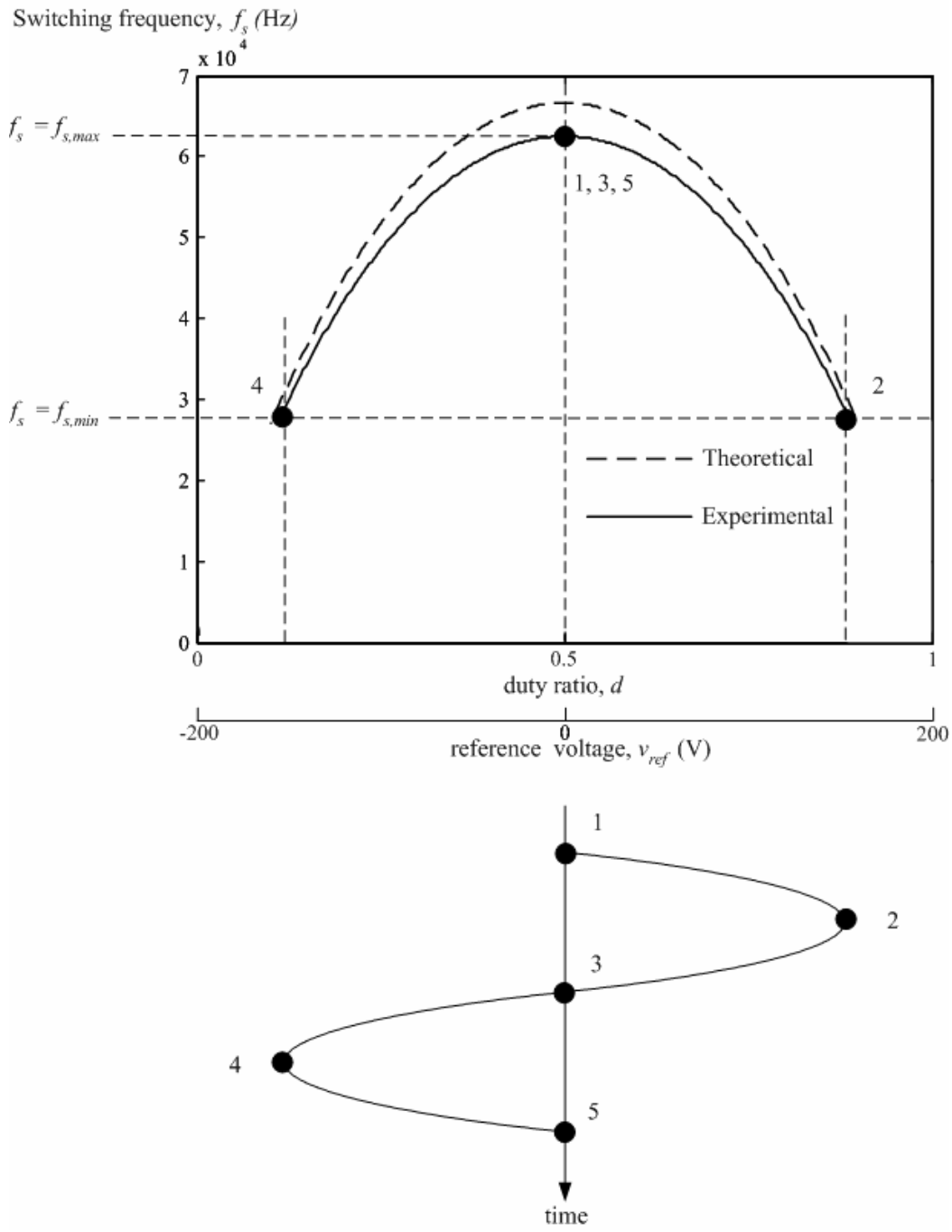


Fig. 4.8 Relationships between f_s and v_{ref} .

4.5 Effects of the Parametric Variations on the Average Output Voltage

As the switching surface parameters k_1 in (4.5) and k_2 in (4.11) are dependent on the values of *L* and *C*. σ^N becomes non-ideal if there is a parametric variation in the values of *L* and *C*. Assume that

$$v_{in} = v_{in,N}(1+\delta_{v_{in}}) \tag{4.36}$$

$$L = L_N(1+\delta_L) \tag{4.37}$$

$$C = C_N(1+\delta_C) \tag{4.38}$$

where $v_{in,N}$, L_N, and C_N are the nominal values of v_{in}, *L* and *C*, respectively, $\delta_{v_{in}}$, δ_L, and δ_C are the fractional changes in v_{in}, *L*, and *C*, respectively.

By substituting (4.36) – (4.38) into (4.31), it can be shown that the maximum output voltage error is equal to

$$\Delta v_{avg} = \left(\left(\frac{2D_N - 1}{2D_N(1-D_N)}\right)\delta_{v_{in}} - \frac{2D_N - 1}{D_N}\delta_L + \frac{2D_N - 1}{D_N}\delta_C + \ldots\right)\Delta_N \tag{4.39}$$

where $D_N = \frac{1}{2}(1+\frac{v_{ref}}{v_{in,N}})$ is nominal duty cycle.

Thus, the output voltage drift has the same sensitivity to the variations in *L* and *C*. The sensitivity is the lowest when D_N equals 0.5 and the sensitivity is the highest when D_N equals 0 or 1. The steady-state output voltage error against the input voltage variation is minimum when D_N = 0.5. Fig. 4.9 shows the output voltage error versus D_N at different percentages of parametric variations. With 50% variation in the three parameters, the output voltage has a maximum error of 2.33% at D_N = 0.1 and 0.9.

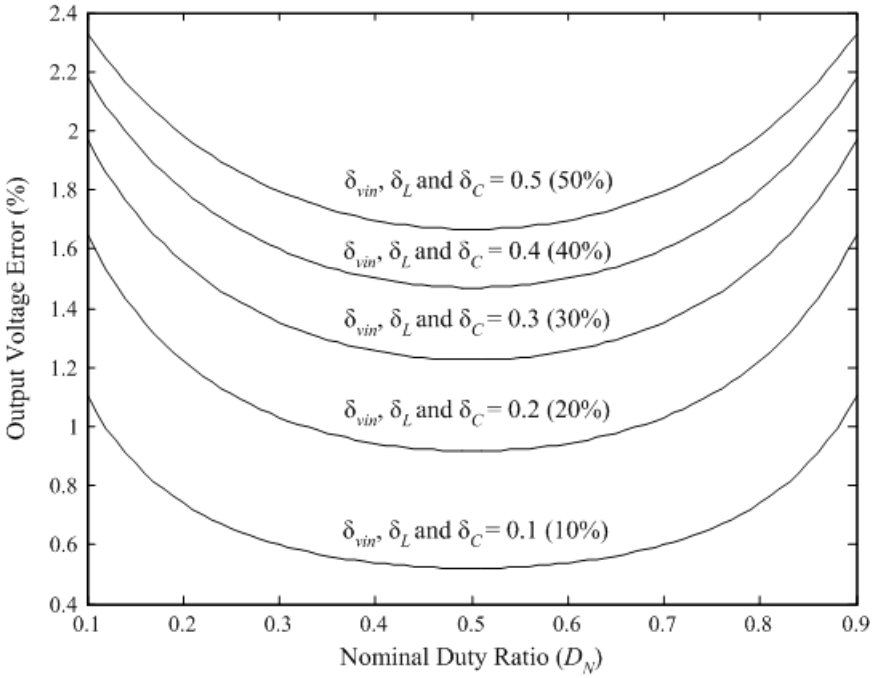


Fig. 4.9 Output voltage error versus duty ratio with different percentages of parametric variations.

4.6 Large-Signal Characteristics

Points along $\sigma^N = 0$ in (4.16) can be classified into refractive, reflective, and rejective modes. The dynamics of the system behaves differently in those regions [Greuel *et al* 1997] and is studied by observing the correlation between the transition boundary and the switching surface. Basically, the value of c_1 in (4.16) determines the dynamic characteristics. Assume that c_1 is a factor of the ideal value of k_1, as defined in (4.5), when S_1 and S_4 are on. That is,

$$c_1 = \zeta_{S_{1,4}}\, k_1 \tag{4.40}$$

where $\zeta_{S_{1,4}}$ is the discrepancy factor. If $\zeta_{S_{1,4}}$ = 1, the inverter follows the derived switching surface. As there are discrepancies between the ideal component values and the actual component values, $\zeta_{S_{1,4}} \neq 1$, resulting in behaving non-ideal dynamic response.

The transition boundary with S_1 and S_4 on is obtained by differentiating (4.16) that

$$R\left[i_L-\frac{v_C}{R}+\left(R\frac{\left(i_L-\frac{v_C}{R}\right)\left(v_{in}+\frac{v_C+v_{ref}}{2}\right)}{v_{in}+v_{ref}}\frac{di_L}{dv_C}\bigg|_{S_{1,4}}-\frac{R}{2}\frac{\left(i_L-\frac{v_C}{R}\right)\left(i_L-\frac{v_{ref}}{R}\right)}{(v_{in}+v_{ref})}\right)\cdot\ln\left(1-\frac{i_L-\frac{v_C}{R}}{\left(R\frac{\left(i_L-\frac{v_C}{R}\right)\left(v_{in}+\frac{v_C+v_{ref}}{2}\right)}{v_{in}+v_{ref}}\frac{di_L}{dv_C}\bigg|_{S_{1,4}}-\frac{R}{2}\frac{\left(i_L-\frac{v_C}{R}\right)\left(i_L-\frac{v_{ref}}{R}\right)}{(v_{in}+v_{ref})}\right)}\right)\right]+(v_C-v_{ref})=0 \tag{4.41}$$

$\left.\frac{d\,i_L}{d\,v_C}\right|_{S_{1,4}}$ in (4.41) is obtained by using (4.1). Thus, equation (4.41) becomes

$$R\left[i_L-\frac{v_C}{R}-\left(\frac{CR}{L}\frac{v_{in}+v_C}{v_{in}+v_{ref}}(v_{in}+\frac{v_C+v_{ref}}{2})+\frac{R}{2}\frac{(i_L-\frac{v_C}{R})(i_L-\frac{v_{ref}}{R})}{(v_{in}+v_{ref})}\right)\cdot\ln\left(1+\frac{i_L-\frac{v_C}{R}}{\left(\frac{CR}{L}\frac{v_{in}+v_C}{v_{in}+v_{ref}}(v_{in}+\frac{v_C+v_{ref}}{2})+\frac{R}{2}\frac{(i_L-\frac{v_C}{R})(i_L-\frac{v_{ref}}{R})}{(v_{in}+v_{ref})}\right)}\right)\right]+(v_C-v_{ref})=0 \tag{4.42}$$

Similarly, the transition boundary with S_2 and S_3 on is obtained by differentiating (4.16) that

$$c_1=\zeta_{S_{2,3}}\,k_2 \tag{4.43}$$

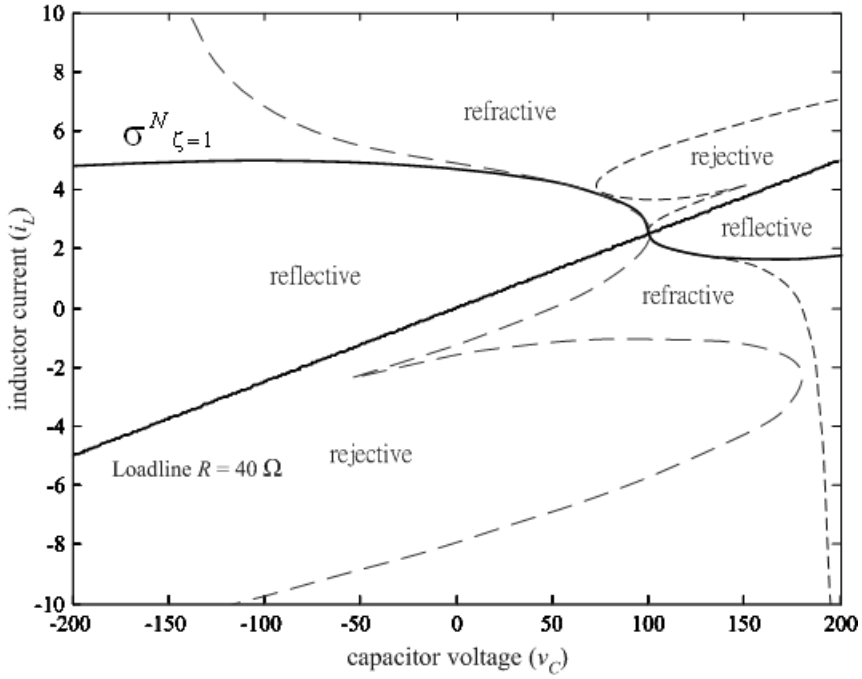
where $\zeta_{S_{2,3}}$ is the discrepancy factor between c_1 and the ideal value of k_2, as defined in (4.11). If $\zeta_{S_{2,3}}$ = 1, the inverter follows the derived switching surface.

$$R\left[\begin{array}{l} i_L-\frac{v_C}{R}+\left(R\frac{\left(i_L-\frac{v_C}{R}\right)\left(v_{in}-\frac{v_C+v_{ref}}{2}\right)}{v_{in}-v_{ref}}\frac{di_L}{dv_C}\Big|_{S_{2,3}}+\frac{R}{2}\frac{\left(i_L-\frac{v_C}{R}\right)\left(i_L-\frac{v_{ref}}{R}\right)}{(v_{in}-v_{ref})}\right) \\ \cdot\ln\left(1-\frac{i_L-\frac{v_C}{R}}{\left(R\frac{\left(i_L-\frac{v_C}{R}\right)\left(v_{in}-\frac{v_C+v_{ref}}{2}\right)}{v_{in}-v_{ref}}\frac{di_L}{dv_C}\Big|_{S_{2,3}}+\frac{R}{2}\frac{\left(i_L-\frac{v_C}{R}\right)\left(i_L-\frac{v_{ref}}{R}\right)}{(v_{in}-v_{ref})}\right)}\right) \end{array}\right] + (v_C-v_{ref})=0 \quad (4.44)$$

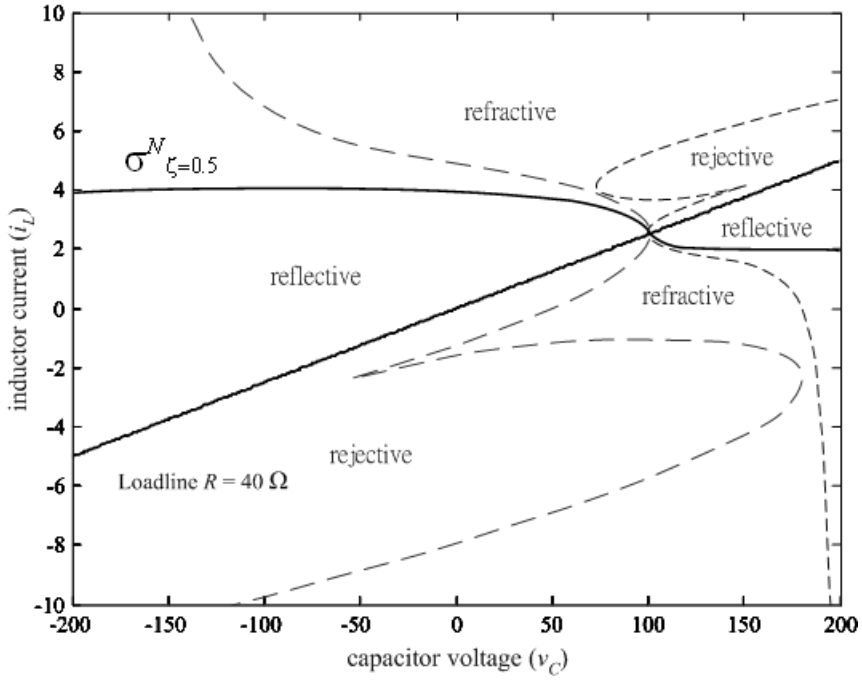
$\left.\frac{d\,i_L}{d\,v_C}\right|_{S_{2,3}}$ is also obtained by using (4.1). Thus, equation (4.44) becomes

$$R\left[\begin{array}{l} i_L-\frac{v_C}{R}+\left(\frac{CR}{L}\frac{v_{in}-v_C}{v_{in}-v_{ref}}(v_{in}-\frac{v_C+v_{ref}}{2})+\frac{R}{2}\frac{(i_L-\frac{v_C}{R})(i_L-\frac{v_{ref}}{R})}{(v_{in}-v_{ref})}\right) \\ \cdot\ln\left(1-\frac{i_L-\frac{v_C}{R}}{\left(\frac{CR}{L}\frac{v_{in}-v_C}{v_{in}-v_{ref}}(v_{in}-\frac{v_C+v_{ref}}{2})+\frac{R}{2}\frac{(i_L-\frac{v_C}{R})(i_L-\frac{v_{ref}}{R})}{(v_{in}-v_{ref})}\right)}\right) \end{array}\right] + (v_C-v_{ref})=0 \quad (4.45)$$

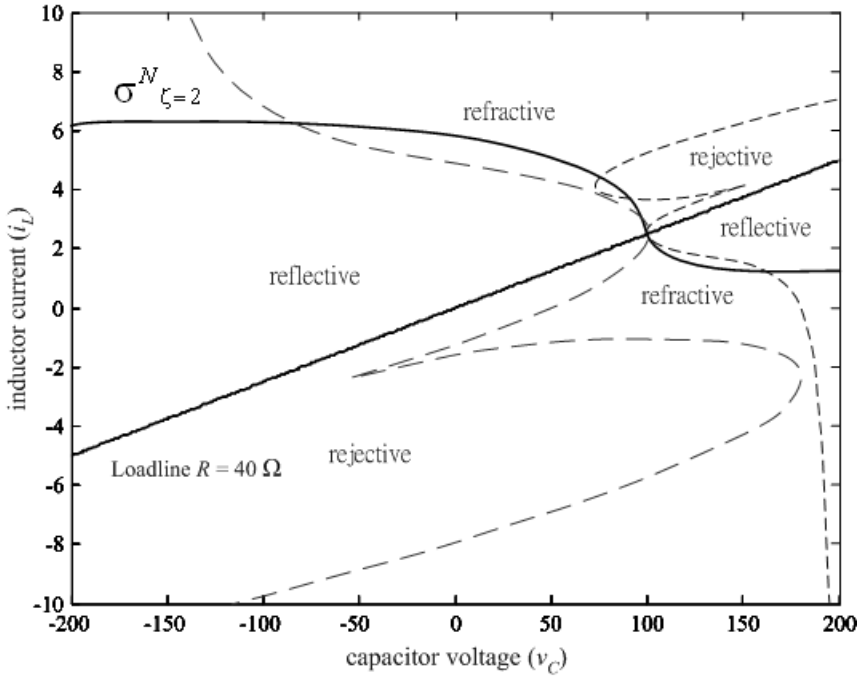
Detailed derivation of (4.42) and (4.45) are given in Appendix.



(a) k_1 and k_2 are ideal ($\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 1$).



(b) k_1 and k_2 are one half of the ideal values ($\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 0.5$).



(c) k_1 and k_2 are twice the ideal values ($\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 2$).

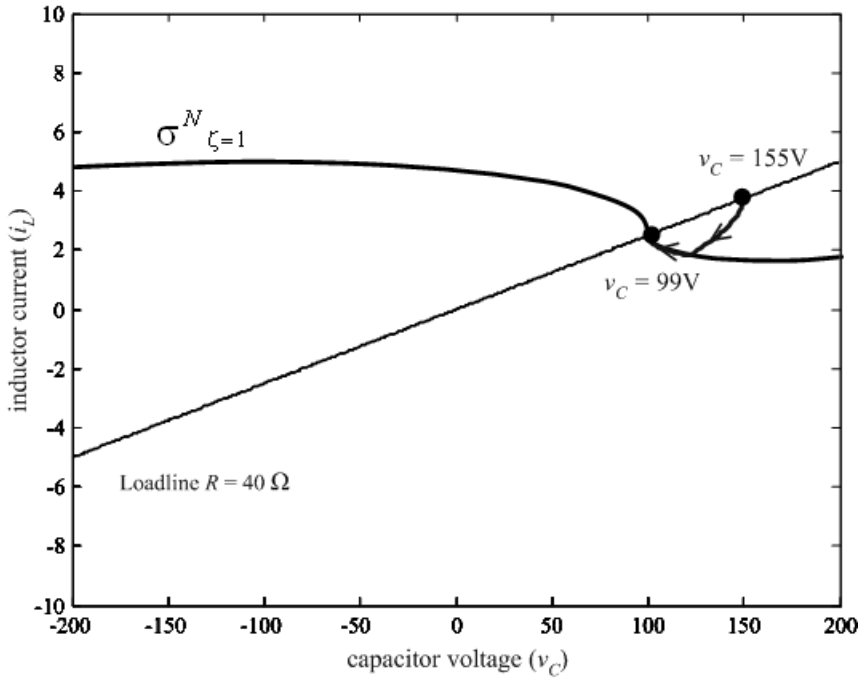
Fig. 4.10 Illustration of the switching surfaces and switching boundaries.

As shown in Fig. 4.10(a), if the values of $\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 1$, the switching surface lies along the transition boundaries and is between the reflective and refractive regions when it is close to the operating point. This leads to good dynamic response to disturbances that the converter will settle to the steady state in two switching actions. However, the switching surface starts deviating from the transition boundaries, when the state point is far from the operating point. This is consistent with the comparison of σ^* and σ^N shown in Fig. 4.5. The inverter will then require more switching cycles to settle under a large-signal disturbance.

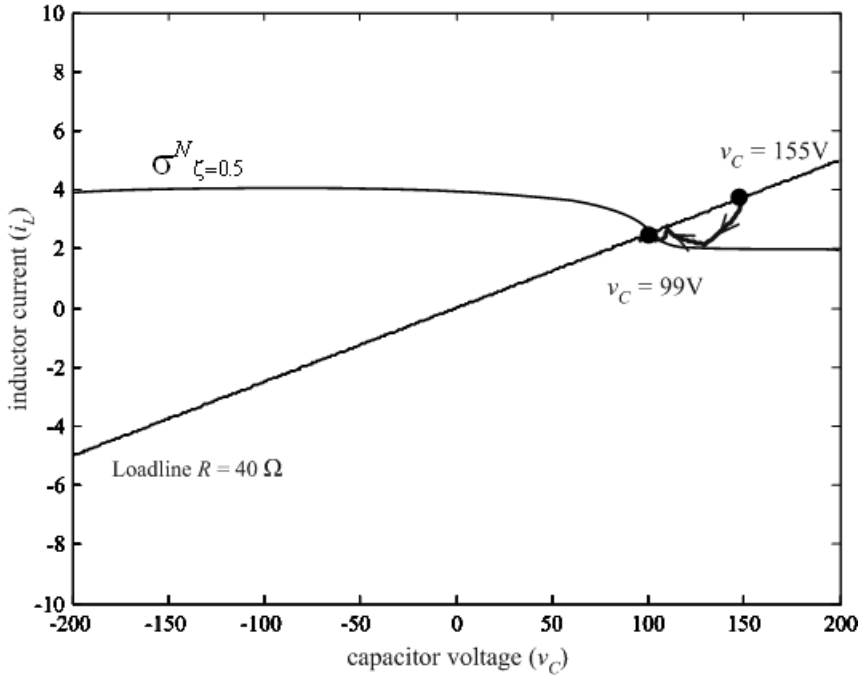
Fig. 4.10(b) shows the transition boundaries and the switching surface with $\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 0.5$. The switching surface almost lies on the reflective region. The implication is that the inverter is operating in sliding mode when it is subject to external disturbance.

Fig. 4.10(c) shows the transition boundaries and the switching surface with $\zeta_{S_{1,4}}$ = $\zeta_{S_{2,3}}$ = 2. The whole switching surface almost lies on the refractive region. The implication is that the inverter's trajectory will move toward the operating point in a spiral manner.

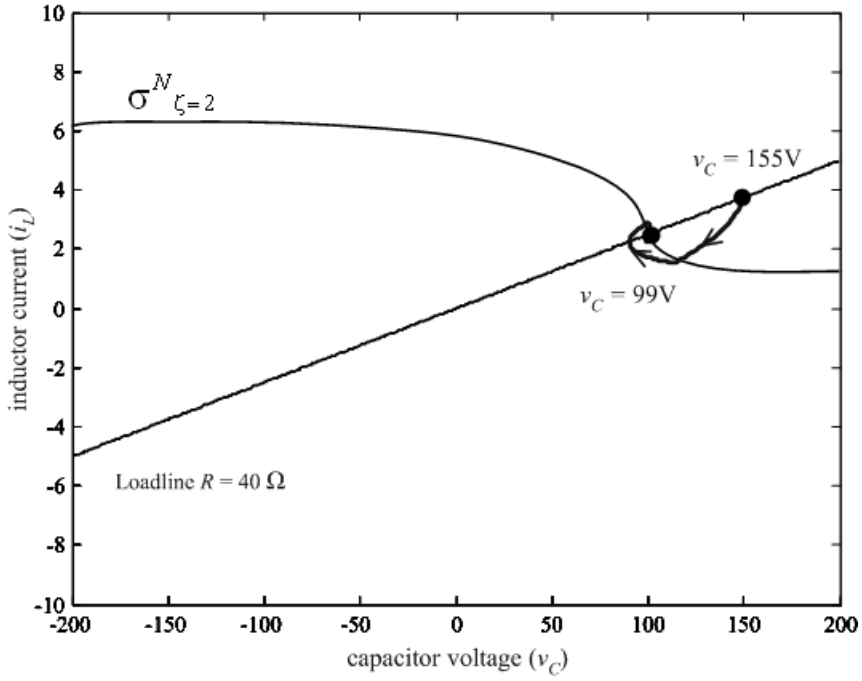
With $\zeta_{S_{1,4}}$ and/or $\zeta_{S_{2,3}}$ not equal to unity, the inverter will requires more switching actions before getting into the steady-state operating point. Fig. 4.11 shows the transient responses of the converter with different values of $\zeta_{S_{1,4}}$ and $\zeta_{S_{2,3}}$. The dynamic behaviors are the best when $\zeta_{S_{1,4}}$ = $\zeta_{S_{2,3}}$ = 1.



(a) k_1 and k_2 are ideal ($\zeta_{S_{1,4}}$ = $\zeta_{S_{2,3}}$ = 1).



(b) k_1 and k_2 are one half of the ideal values ($\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 0.5$).



(c) k_1 and k_2 are twice the ideal values ($\zeta_{S_{1,4}} = \zeta_{S_{2,3}} = 2$).

Fig. 4.11 Simulated state-space trajectories of the inverter various k_1 and k_2 with the switching boundaries.

4.7 Experimental Verifications

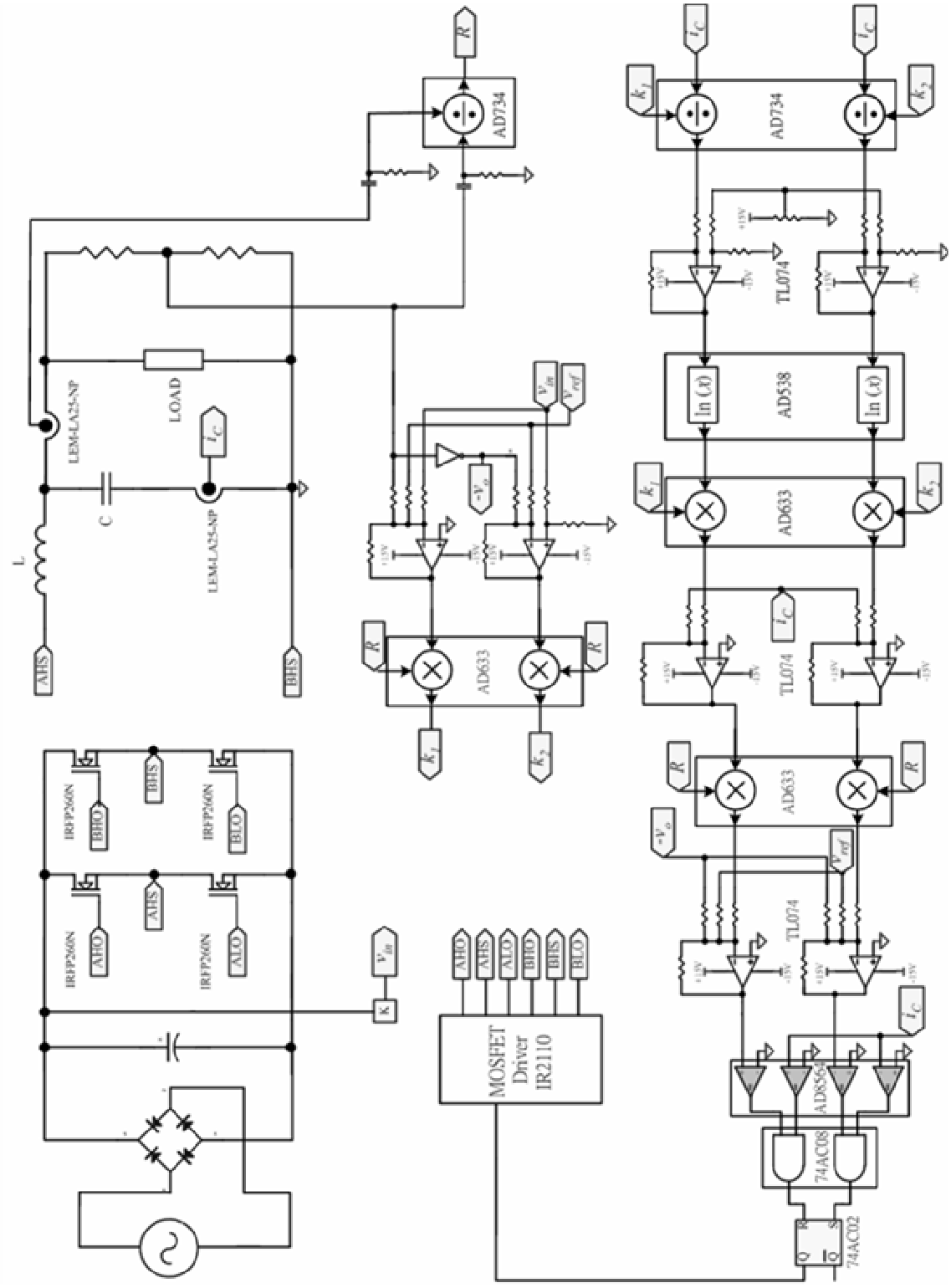
A 300W, 110V, 60Hz full bridge inverter has been built and tested. The schematic of the circuit is shown in Fig. 4.12(a). The component values are tabulated in Table I. As shown in Appendix, the filter is designed to make it operate at the critical damping condition and rated power condition. As the power rating is 300W and the voltage rating is 110V, $Z = 40\Omega$. The cutoff frequency f_C of the filter, which is chosen to be one-fourth of the minimum switching frequency of 25kHz, equals 6.3kHz. By putting Z and $\omega_n = 2\pi f_C$ into (A.1) and (A.2), the values of L and C shown in Table 4.1 are calculated.

Fig. 4.13 shows the enlarged waveforms of the dynamic responses of the inverter supplying to the 40Ω resistive load with different switching surfaces, including σ^N, σ^2 and σ^1. The reference voltage is suddenly changed at the peak of the reference signal from $70V_{rms}$ to $110V_{rms}$. The transient periods of the inverters with σ^1, σ^2, and σ^N are 75μs, 73μs, and 35μs, respectively. Among them, σ^N gives the best dynamic response. As shown in Fig. 4.13(c), the inverter only takes two switching actions getting into the steady state. The output voltage looks constant before and after the disturbance, because the timebase of measurement is 40μs and is much shorter than the period of the output voltage, which is 1/60Hz = 16.67ms. The variation of the output voltage is thus very small.

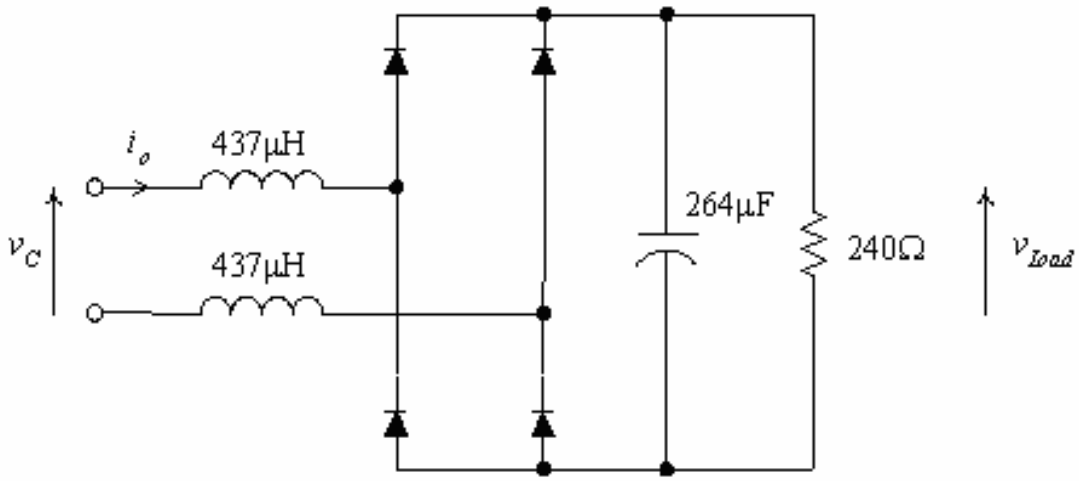
Fig. 4.14 shows the steady-state output voltage waveforms supplying to resistive, nonlinear inductive, and full-wave rectifier loads. The output voltage is sinusoidal in all cases. The load specifications are tabulated in Table 4.2. The schematic of the full-wave rectifier load is shown in Fig. 4.12(b). Fig. 4.15 shows the steady-state waveforms when the dc input voltage has fluctuation of 10%. The purpose is to simulate the condition that the dc rail is derived by rectifying the ac voltage shown in Fig. 4.12(a) and the proposed method can still provide a sinusoidal waveform with low

total harmonic distortion (THD). It should be noted here that similar steady-state waveforms can be obtained with σ^1 and σ^2, because all three switching surfaces are close to σ^* around the operating point (Sec. III). However, σ^N gives better large-signal dynamic responses.

Fig. 4.16 shows the harmonic spectra of the output voltage with different loads. The third harmonics (180Hz) is less than the fundamental component (60Hz) by more than 45dB in both cases. The THD of the output voltage is less than 1.1%. Fig. 4.17 shows the transient responses of the output voltage when the resistive load is changed from the rated load to 20% load, and vice versa. The inverter can revert to the steady state in two to three switching actions. As explained in Sec. VI, the required switching action is more than two if the inverter state point is far from the steady-state operating point. Nevertheless, the inverter output voltage can still get into the 3% band within two switching actions. Thus, apart from providing fast dynamic response, the proposed control method can equally give good output harmonic spectra in inverter applications.

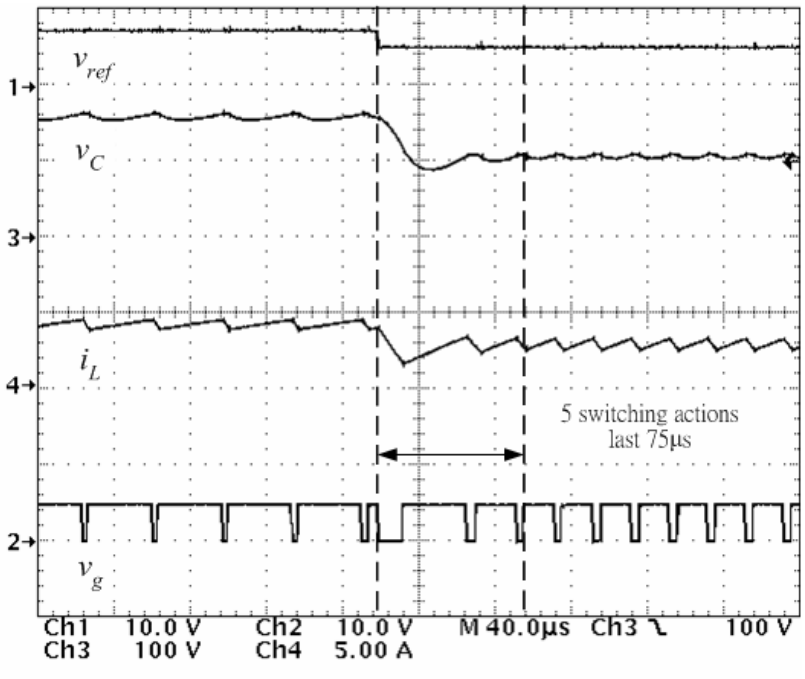


(a) Schematic of the prototype.

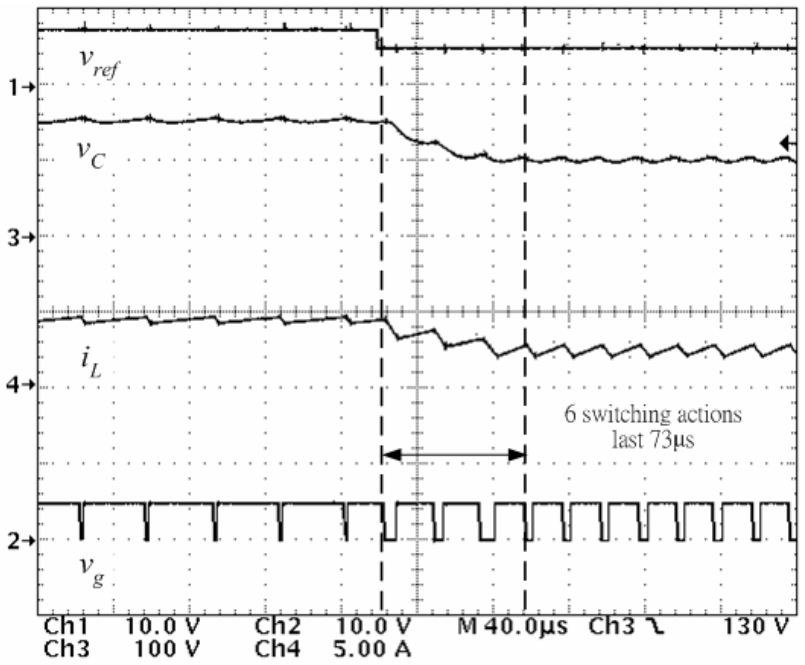


(b) Schematic of the full-wave rectifier load.

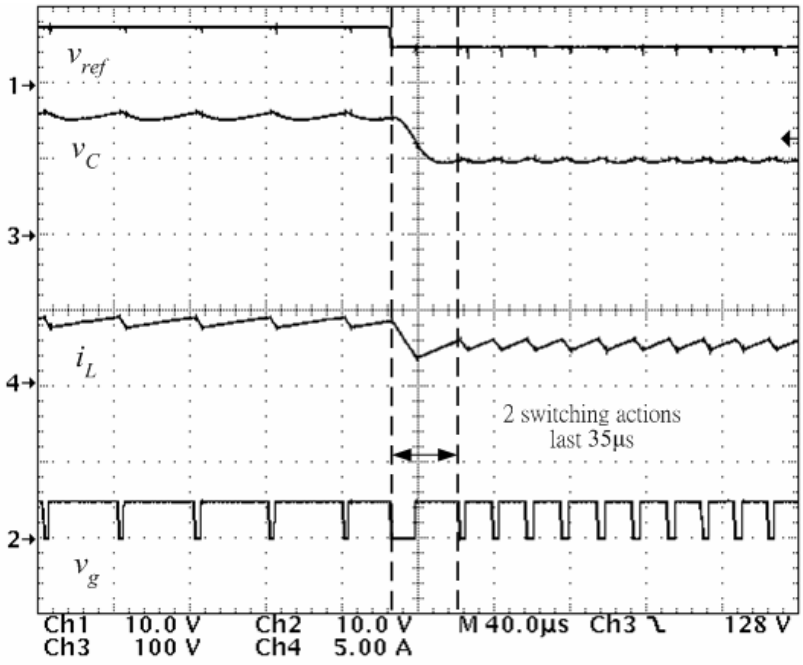
Fig. 4.12 Hardware implementation.



(a) σ^1.

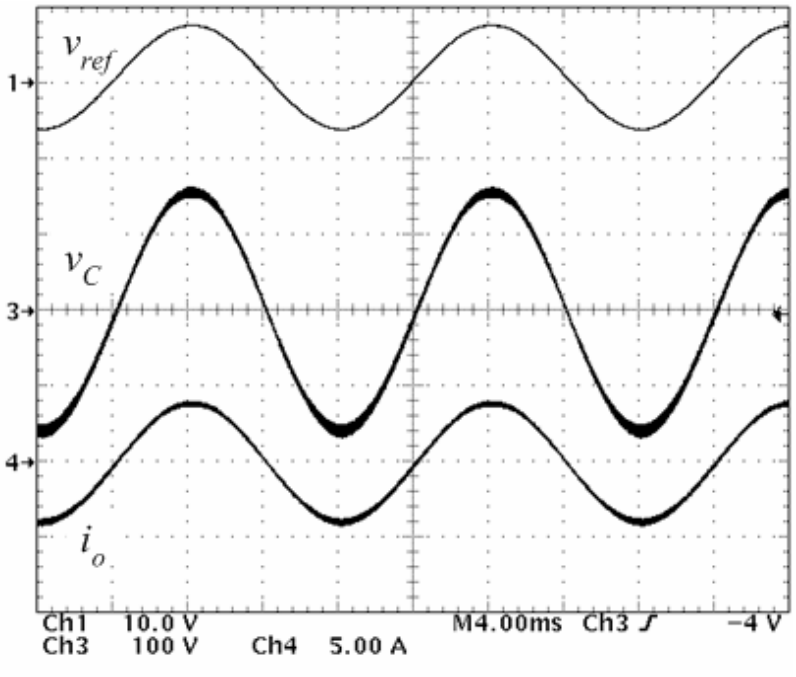


(b) σ^2.

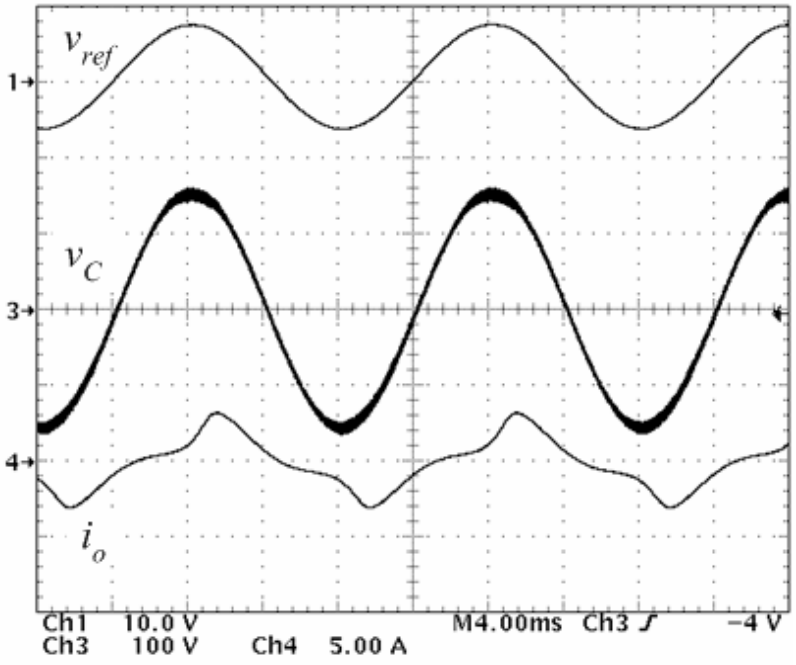


(c) σ^N.

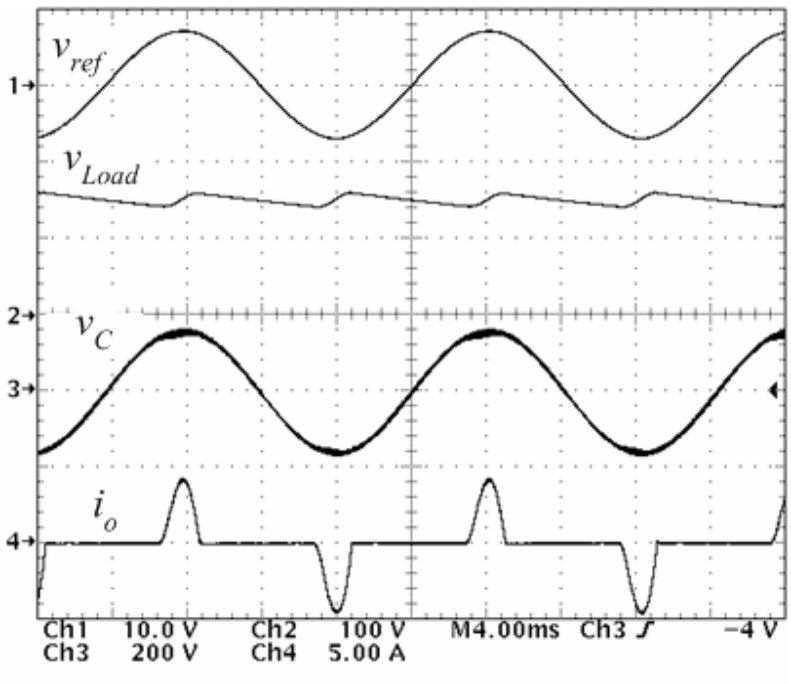
Fig. 4.13 Dynamic response of the inverter when the reference signal is changed from 110 V_{rms} to 70 V_{rms} at the angle around 90˚ [Ch1: v_{ref} (10 V/div), Ch2: v_g (10 V/div), Ch3: v_C (100 V/div), Ch4: i_L (5 A/div), timebase: 40µs/div].



(a) Resistive load.

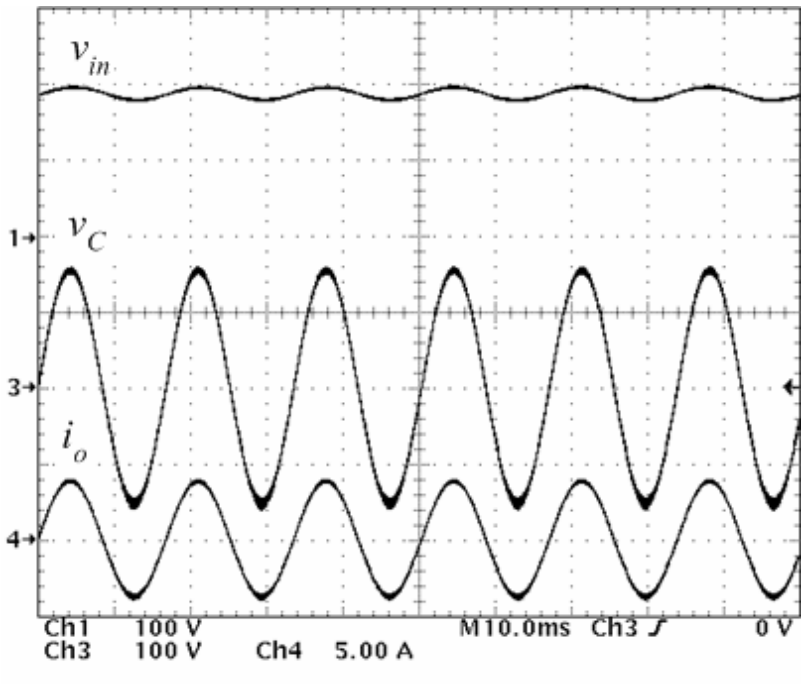


(b) Non-linear inductive load.

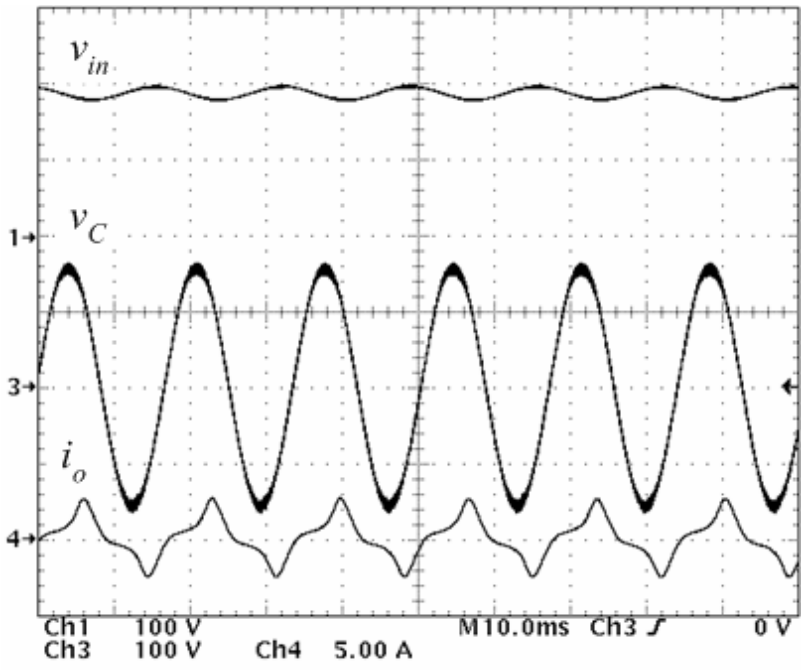


(c) Full-wave rectifier load.

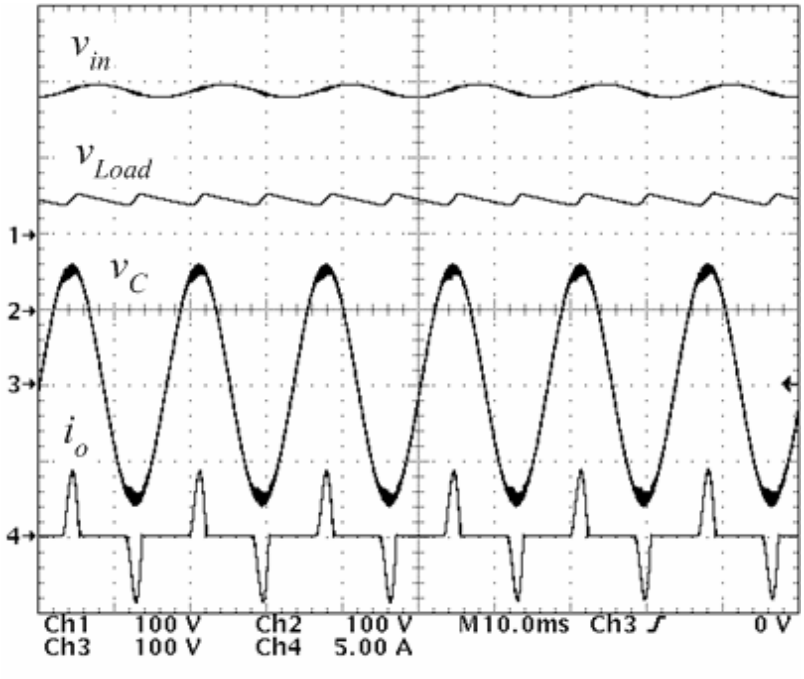
Fig. 4.14 Steady-state operations of the inverter [Ch1: v_{ref} (10 V/div), Ch2: v_{Load} (100V/div), Ch3: v_C (100 V/div), Ch4: i_o (5 A/div), timebase: 4ms/div].



(a) Resistive load.

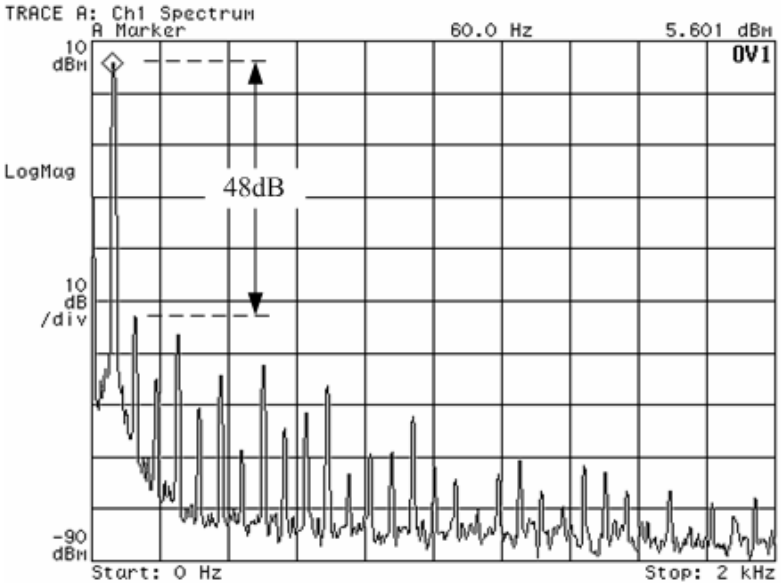


(b) Nonlinear inductive load.

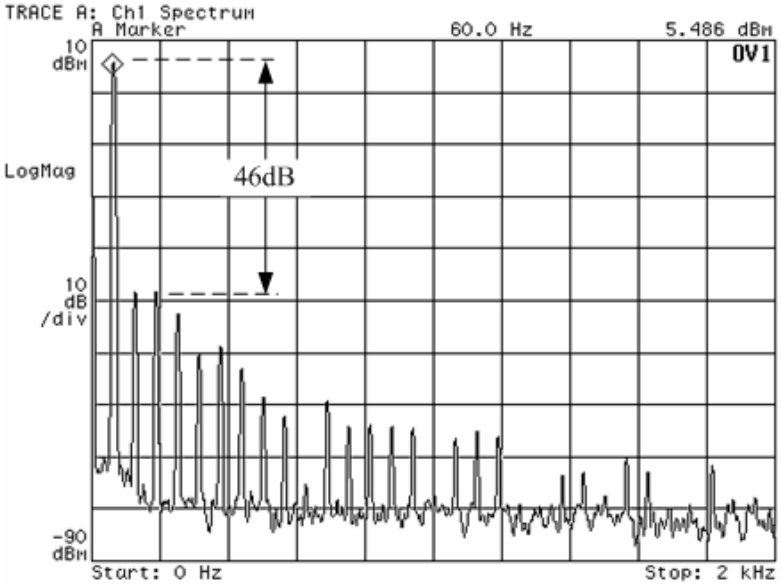


(c) Full-wave rectifier load.

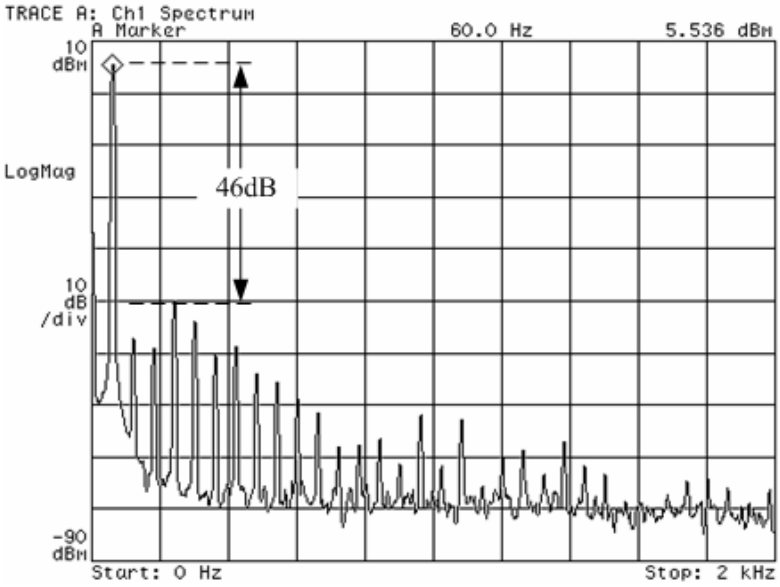
Fig. 4.15 Steady-state operation with 10% input voltage variation [Ch1: v_{in} (100 V/div), Ch2: v_{Load} (100V/div), Ch3: v_C (100 V/div), Ch4: i_o (5 A/div), timebase: 10ms/div].



(a) Resistive load.

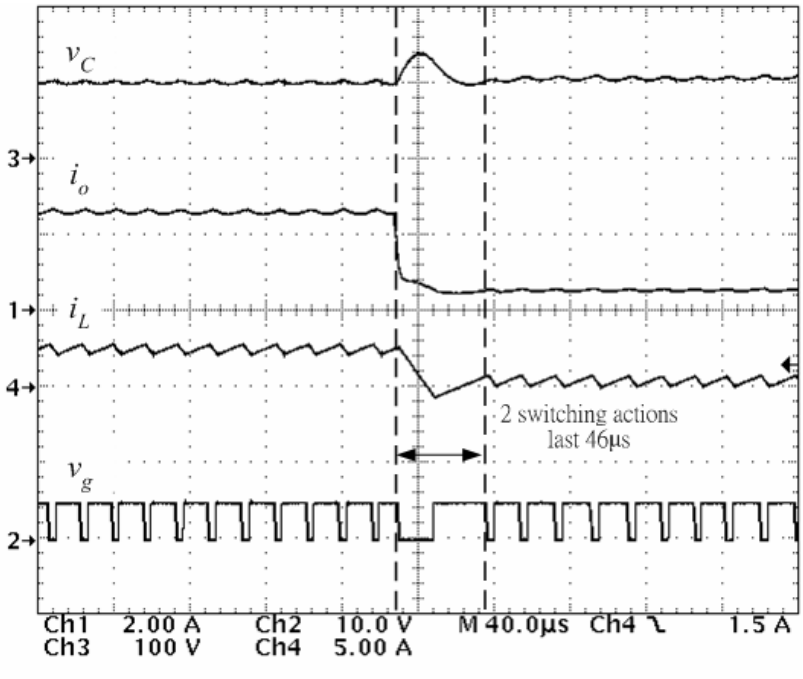


(b) Nonlinear inductive load.

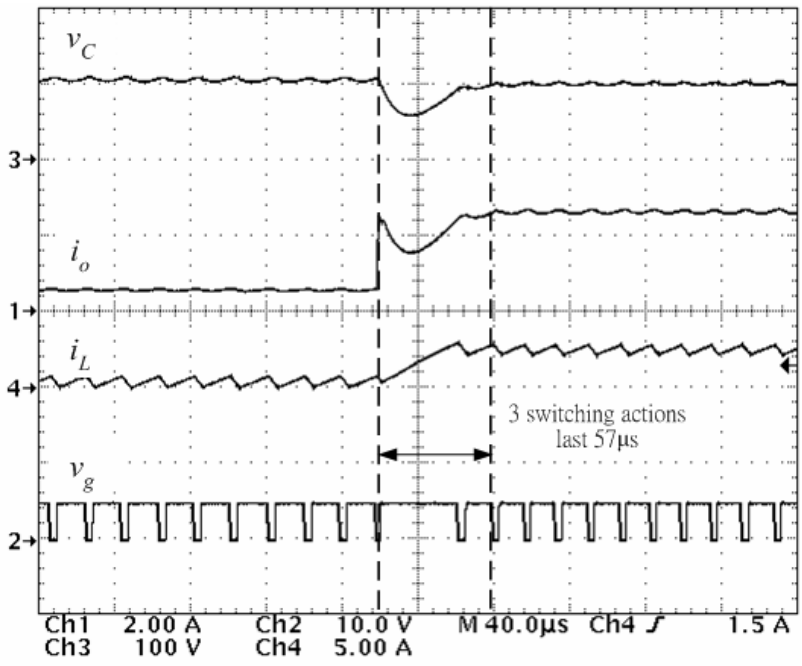


(c) Full-wave rectifier load.

Fig. 4.16 Harmonic spectra of the output voltage.



(a) Rated load to 20% load.



(b) 20% load to rated load.

Fig. 4.17 Transient responses under load changes [Ch1: i_o (2 A/div), Ch2: v_g (10 V/div), Ch3: v_C (100 V/div), Ch4: i_L (5 A/div), timebase: 40µs/div].

Table 4.1 Component used in the simulation and prototype

Parameter	Value
v_{in}	200 V
L	2mH
C	320nF

Table 4.2 Load specification of the prototype

Load (Z)	Value
Resistive	40Ω
Nonlinear Inductive	23mH + 40Ω
Full-wave rectifier load	264μF + 240Ω

Table 4.3 Comparison of the settling times with different switching surfaces

Switching surface	Settling time (μs)	
	From 70Vrms to 110Vrms	From 110Vrms to 70Vrms
σ^1	48.8	46.9
σ^2	42.7	46.9
σ^N	21.9	46.9

4.8 Chapter Summary

A high-order switching surface for boundary control of inverters has been presented. It has also been shown that the first- and second-order switching surfaces are the low-order approximation of σ^N. The control method does not require any sophisticated calculations of the transfer functions or closed-loop compensation. The controller's parameters are obtained readily by considering the component values of the power stage. It is unnecessary to determine the controller parameters by the trail-and-

error approach. Most importantly, the control method is for large-signal control. The proposed method has been confirmed experimentally. Further research will be dedicated into the boundary control with constant switching frequency.

4.9 Appendix

4.9.1 Derivation of Z_C in (4.24)

As shown in [Nise 1995], the transfer function $G(s)$ of the output filter is a second-order system. It can be shown that

$$G(s) = \frac{v_C(s)}{v_x(s)} = \frac{\omega_n^{\,2}}{s^2 + 2\,\xi\,\omega_n\,s + \omega_n^{\,2}} \tag{A4.1}$$

where $\omega_n = \sqrt{\frac{1}{L\,C}}$ and $\xi = \frac{1}{2\,C\,Z\,\omega_n}$ are the natural frequency and damping ratio of the filter, respectively.

The filter will be in critical damping (i.e., $\xi = 1$) when

$$Z = Z_C = \frac{1}{2}\sqrt{\frac{L}{C}} \tag{A4.2}$$

4.9.2 Derivations of (4.41), (4.42), (4.44), and (4.45)

Substitute $c_1 = \zeta_{S_{1,4}}\, k_1 = \zeta_{S_{1,4}} \frac{CR}{L}(-v_{in} - \frac{v_C + v_{ref}}{2})$ into (4.16) with $\sigma^N = 0$,

$$R\left[\begin{array}{l} i_C + \zeta_{S_{1,4}} \dfrac{CR}{L}\left(-v_{in} - \dfrac{v_C + v_{ref}}{2}\right) \\ \cdot \ln\left(1 - \dfrac{i_C}{\zeta_{S_{1,4}} \dfrac{CR}{L}\left(-v_{in} - \dfrac{v_C + v_{ref}}{2}\right)}\right) \end{array}\right] + (v_C - v_{ref}) = 0 \tag{A4.3}$$

Then, by differentiating both sides of (A4.3), it gives

$$\zeta_{S_{1,4}} = -\frac{L}{C}\frac{i_L - \frac{v_C}{R}}{v_{in} + v_{ref}}\frac{di_L}{dv_C}\bigg|_{S_{1,4}} + \frac{L}{2C}\frac{\left(i_L - \frac{v_C}{R}\right)\left(i_L - \frac{v_{ref}}{R}\right)}{\left(v_{in} + \frac{v_C + v_{ref}}{2}\right)\left(v_{in} + v_{ref}\right)} \tag{A4.4}$$

Equation (4.41) can then be derived by substituting the value of (A4.4) into (A4.3).

Similarly, substitute $c_1 = \zeta_{S_{2,3}}\ k_2 = \zeta_{S_{2,3}} \frac{CR}{L}(v_{in} - \frac{v_C + v_{ref}}{2})$ into (4.16) with $\sigma^N = 0$,

$$R\left[\begin{array}{l} i_C + \zeta_{S_{2,3}} \dfrac{CR}{L}\left(v_{in} - \dfrac{v_C + v_{ref}}{2}\right) \\ \cdot \ln\left(1 - \dfrac{i_C}{\zeta_{S_{2,3}} \dfrac{CR}{L}\left(v_{in} - \dfrac{v_C + v_{ref}}{2}\right)}\right) \end{array}\right] + (v_C - v_{ref}) = 0 \qquad \text{(A4.5)}$$

Again, by differentiating both sides of (A4.5)

$$\zeta_{S_{2,3}} = \frac{L}{C} \frac{i_L - \frac{v_C}{R}}{v_{in} - v_{ref}} \left.\frac{di_L}{dv_C}\right|_{S_{2,3}} + \frac{L}{2C} \frac{\left(i_L - \frac{v_C}{R}\right)\left(i_L - \frac{v_{ref}}{R}\right)}{\left(v_{in} - \frac{v_C + v_{ref}}{2}\right)\left(v_{in} - v_{ref}\right)} \qquad \text{(A4.6)}$$

Equation (4.44) can then be derived by substituting the value of (A4.6) into (A4.5).

Based on (4.1),

$$\left.\frac{di_L}{dv_C}\right|_{S_{1,4}} = -\frac{C}{L} \frac{v_{in} + v_C}{i_L - \frac{v_C}{R}} \qquad \text{(A4.7)}$$

$$\left.\frac{di_L}{dv_C}\right|_{S_{2,3}} = \frac{C}{L} \frac{v_{in} - v_C}{i_L - \frac{v_C}{R}} \qquad \text{(A4.8)}$$

By putting (A4.7) and (A4.8) into (4.41) and (4.44), respectively, eq. (4.42) and (4.45) can be obtained.

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS FOR FURTHER RESEARCH

5.1 Conclusions

This thesis has proposed three main ideas in order to obtain low output harmonic distortion in control of switch-mode inverters. The concept of the proposed ideas is divided into two categories, the power stage and the controller stage.

The idea of transient dc-link boost technique has been proposed for eliminating the eventuality of pulse-dropping phenomenon for the consideration in power stage. Apart from effectively reducing harmonic distortion at the output, the proposed method can also widen the dynamic modulation range and thus reduce the required supply voltage. The effectiveness of the method has been supported by experimental measurements.

The use of second-order switching surface for boundary control of switch-mode inverter has been proposed with the consideration in controller stage. The control method is simple and does not require any complicated calculation of the system transfer function or control loop compensation. The output voltage can obtain near-optimal response when it is subject to large-signal disturbances or input voltage variation. The control method has been studied experimentally with a 100 W inverter prototype and provides good agreement with theoretical prediction.

A high-order switching surface for boundary control of inverters has been proposed. It has also been shown that the first- and second-order switching surfaces are the low-order approximation of σ^N. The controller's parameters are obtained readily by considering the component values of the power stage. It is unnecessary to determine the controller parameters by the trail-and-error approach. Most importantly, the control method is for large-signal control. The proposed method has been confirmed experimentally.

Major contributions and results of this thesis are summarized as follows. Suggestions for further research are described in the next section.

5.2 Major Contributions

The major contributions to the second-order switching surface in boundary control can be summarized to the following aspects.

(i) Developed the concept of transient dc-link boost to avoid pulse-dropping phenomenon in the power stage of inverters.

(ii) Applied the concept of second-order switching surface of boundary control in inverters.

(iii) Developed the concept of high-order switching surface of boundary control for inverters.

(iv) Studied the steady-state and large-signal characteristics of the inverter with high-order switching surface.

5.3 Suggestions for Further Research

5.3.1 High-order Switching Surface for Boundary Control with Fixed-Switching frequency

With the use of second- or high-order switching surface for boundary control of inverters, the switching frequency is varied with respect to the reference voltage. Thus, the variation of the switching frequency will lead to electromagnetic perturbation and filter designation problems. It can be solved by increasing the input voltage in order to reduce the ratio of the maximum reference voltage to the input voltage. However, the utilization of the input voltage has been reduced. Some researchers proposed alternative designs which combine the robustness of sliding mode control with constant

switching frequency. By the use of variable hysteresis band [Ruiz *et al* 1990; Chiarelli 1993; Malesani 1996b] or injecting a fixed frequency signal to the switching surface [Silva 1993; Pinheiro 1994; Nicolas 1996], the purpose of fixed switching frequency can be achieved. However, the transient responses are not optimum in those cases. To conclude, a control with fixed switching frequency and optimum transient response is the aim of the task, and high-order switching surface for boundary control with fixed-switching frequency will be further investigated.

PUBLICATIONS FROM THIS THESIS

Journal / Transaction Papers

[1] Kelvin K. S. Leung, Julian Y. C. Chiu and Henry S. H. Chung, "Boundary Control of Inverters Using Second-Order Switching Surface", *IEEE Transactions on Power Electronics*. (Submitted)

[2] Julian Y. C. Chiu, Kelvin K. S. Leung and Henry S. H. Chung, "High-Order Switching Surface in Boundary Control of Inverters", *IEEE Transactions on Power Electronics*. (Accepted for publication)

Conference Papers

[3] Y. C. Chiu, B. Zhou, Henry S. H. Chung and W. H. Lau, "The Implementation of Transient DC-link Boost Based Digital Amplifier for Eliminating Pulse-Dropping Distortion," *in Proc. IEEE International Symposium on Circuit and Systems* (ISCAS), May 2004, pp. 864-867.

[4] B. Zhou, Y. C. Chiu, W. H. Lau and Henry S. H. Chung, "Spectral Analysis of A Novel Transient Dynamic Boost PWM Inverter Control for Power Amplifiers," *in Proc. IEEE International Symposium on Circuit and Systems* (ISCAS), May 2004, pp. 876-879.

[5] Kelvin K. S. Leung, Julian Y. C. Chiu and Henry S. H. Chung, "Boundary Control of a Bipolar Square-Wave Generator Using Second-Order Switching Surface", *in Proc IEEE International Symposium on Circuits and Systems* (ISCAS), May 2005, pp. 3079-3082.

[6] Kelvin K. S. Leung, Julian Y. C. Chiu and Henry S. H. Chung, "Boundary Control of Inverter Using Second-Order Switching Surface", *in Proc. IEEE 36th Power Electronics Specialists Conference* (PESC), June 2005, pp. 936-942.

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