City University of Hong Kong

香港城市大學

Controlled Doping in CdSe Nanowires: Synthesis, Characterization and Devices Applications

硒化鎘納米綫的可控摻雜：合成、表徵及器件的研究

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By
HE Zhu-Bing
何祝兵

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Abstract

CdSe is an important group II-VI direct band gap (visible) semiconductor material with attractive electronic, spintronics and optoelectronic properties. It has shown great potential in the applications, such as biosensing/bioimaging, light emitting diode, and photodetectors. Although CdSe Nanowires (NWs) are very promising building blocks for the applications mentioned above, some inevitable obstacles remain for the practical application of CdSe NWs based *nano*-optoelectronic devices. First, controllable and uniform doping in CdSe NWs is the critical prerequisite in semiconducting applications. Second, how to define these NWs to a desired position with reasonable reliability and reproducibility, or how to construct these building blocks into the desired structure, is a technique to be developed. Third, the influences of NWs surface, contact between NWs and electrodes, interface between NWs and package films on the electronic transportation properties are not well understood yet. Last but not the least, how to enhance the performance of the whole device based on these nanomaterials is predominant in devices applications.

In this thesis, controlled doping in CdSe NWs and optimization of devices based on them are systematically studied. Indium doping in CdSe NWs via two approaches, ie., i) in-situ co-evaporation of both CdSe and indium powder source in a thermal transport system, ii) doping via post annealing of CdSe NWs in indium vapor, were successfully demonstrated for the first time. The methods were found to be effective and the transport properties of CdSe NWs were tuned to vary over a wide range. The conductivity of CdSe NWs was increased by nearly five orders of the magnitude from ~10^{-4} to tens Scm^{-1} by the doping, and the carrier concentration as high as ~10^{19} cm^{-3} was achieved for the heaviest

doping. The doped CdSe NWs showed a high sensitivity to light irradiation. Prolonged decay edges for the heavily doped CdSe NWs were observed, which were attributed to increased trapping centers arising from an increasing indium concentration.

Although we achieved uniform CdSe NWs with controlled doping concentration, the gate effect of transistors based on single CdSe:In NWs did not fully meet the expectation, owing to the inherent disadvantage of the structure of these field effect transistors (FETs). Herein, high-performance CdSe:In nanowire FETs using high k Al_2O_3 as the gate insulator is reported. A simple technique that involved rapid thermal annealing the prepared Al metallic gate was employed to fabricate the ultrathin Al_2O_3 gate layer. In contrast to the devices constructed on conventional SiO_2/Si substrate, the CdSe:In nanowire FETs with Al_2O_3 gate show considerate improvement in device performances, such as large transconductance and enhanced current switching characteristics. In addition, this developed method has been proven to be compatible with flexible substrates which thus open the opportunities for the applications of nano-FETs in flexible electronics.

Moreover, the performance gain of transistor based on single doped CdSe NWs is also augmented by substituting the planar back gate by the top gate geometry with another high k dielectric material, Si_3N_4, as discussed in chapter 4. A systematic study of the gate performance of the top gate and back gate FET based on the same single indium doped CdSe nanowire (NW), using Si_3N_4 and SiO_2 as gate dielectric materials, respectively was conducted. The I_{on}/I_{off} ratio and field effect mobility of the top gate transistor reached over 10^5 and 166 cm^2/V s, respectively. The threshold voltage and the subthreshold swing were reduced to -1.7 V and 508 mV/dec. The performance was the most exceptional ever reported for CdSe and even II-VI semiconductor nanomaterial based devices. Both the high κ gate material, Si_3N_4, and the gate geometry contribute most to a significant enhancement of the performance of FET devices. Based on the good performance of these top gate transistors alone, two basic logic gates, 'AND' and 'OR', were fabricated and a rapid and stable switch effect was shown. These logic gates can also be functionalized by common white lamp light owing to the good photoconductivity of CdSe.

We also studied electronics properties of heretrojuncts between *n*- type CdSe:In NWs and *p*- type silicon nanoribbon (NRs). Patterned *p*- type Si NRs were fabricated using reactive ion etching (RIE) of SOI substrate. By positioning the doped *n*- type CdSe NWs just crossing each as-etched silicon NR by electrical field, heterjunctions array with these *n*-type CdSe NWs and *p*- type silicon nanoribbon (NRs) were formed. These heterojunctions exhibit multi-functionalities, including *p*-*n* diode with small turn-on voltage (0.5~2 V) and large breakdown voltage (over 30V), Junction FETs (JFETs) and possible light emission diode (LED). These JFETs demonstrate superior performance to single CdSe:In NW based back gate metal oxide semiconductor FETs (MOSFETs) in transconductance, I_{on}/I_{off} ratio, threshold voltage, substhreshold swing and so on. The conductance of the CdSe:In NW channel can be changed by a factor of more than 10^3 with only -2 to -1V variation in the *p*-*n* junction gate. We attribute the high sensitivity of the JFETs to outstanding channel tuning effects of the new type nano *p*-*n* junction gate diode. For LED, it is believed that this work would serve as a catalyst to construct red pixels, as well as study of light emission mechanisms at the CdSe and Si interface.

Additionally, the controllable indium in-situ doping can be utilized in other II-VI semiconductors nanostructures such as ZnSe NWs. The doping concentration variation and derived morphology evolution of ZnSe:In NWs are discussed. For unintentionally doped

ZnSe NWs, the surface of NWs is smooth and the cross-section is rectangular. In contrast, the surface changes coarsely and even into hierarchy structures, and the cross-section evolves from a square to circular and eventually to irregular polygon, which are attributed to the indium vapor in the growth system. The indium concentration varies from undetectable to near 10 at% in a single NW electron diffraction X-ray spectrum. The result proves that this in-situ doping method can be a general method for doping of II-VI semiconductor 1D nanomaterials.

The series of efforts mentioned above were dedicated to study some basic electronic and optoelectronic properties of doped CdSe NWs, and also to explore some exciting and promising performance of *nano*- devices based on them at an incipient stage. We believe that these works would serve as a catalyst for future research on CdSe and relative II-VI semiconductor nanomaterials based *nano*- optoelectronic and electronic devices.

List of figures

FIG. 1.4. Schematic illustration (Left) of vapor-liquid-solid nanowire growth mechanism including three stages alloying, (II) nucleation, and (III) axial growth. The three stages are projected onto the conventional Au-Ge binary phase diagram to show the compositional and phase evolution during the nanowire growth process. The right pictures show the real time growth course of a Ge NW. Reprinted with permission from ACS.

FIG. 1.5 A typical schematic illustration of SLS growth mechanism of nanowires (top). A-D (down): TEM images of high crystalline Si NWs yielded in the SLS mechanism. Reprinted with permission of Science Group.

FIG. 1.6 Monomer concentration dependent growth paths of CdSe nanocrystals. Reprinted with permission of John-Wiley.

FIG. 1.7 a) Energy level diagram of a bilayer device composed of a thin layer of CdSe NCs and PPV film. b) CdSe NCs size dependent PL and EL emission of the devices. c) Voltage dependent color of the bilayer device. Reprinted with permission from Science Group.

FIG. 1.8. a) I–V behavior of n–n, p–p, and p–n junctions of crossed n- and p-InP nanowires. The green and blue curves correspond to the I–V behavior of individual n- and p-type nanowires in the junction, respectively. The red curves represent the I–V behavior across the junctions. Reproduced with permission from Nature Publishing Group.[50] b) EL spectra from crossed *p–n* diodes of *p*-Si and *n*-CdS, CdSSe, CdSe, and InP (top to bottom, respectively). Insets to the left are the corresponding EL images for CdS, CdSSe, CdSe, and InP nanowire LEDs. The top-right inset shows representative I–V and SEM data recorded for a *p*-Si/*n*-CdS crossed NW junction (scale bar 1mm). c) Schematic and corresponding SEM image of a tricolor nano-LED array. d) Normalized EL spectra and color images from the three elements. Reproduced with permission from John-Wiley.

Black solid blocks and blue hollow blocks correspond to linear scale and log scale I_{ds}-V_{ds} curve, respectively. (c) and (d) The leakage current between gate electrode and NW channel, and the characteristic of μ_{eff}-V_{gs} of the top gate FET, respectively.

FIG. 4.4. (a) Configuration of a single CdSe:In NW-based back-gate FET using 100 nm sputtered Si_3N_4 film as gate dielectric. (b) I_{ds}-V_{ds} curve of the FET with gate voltages ranging from –9 to 12V in step of 3V. (b) The I_{ds}-V_{gs} curve characteristics of the FET at V_{ds}=1 V. Black solid blocks and blue hollow blocks correspond to linear scale and log scale I_{ds}-V_{ds} curve, respectively.

FIG. 4.5. (a) Hysteresis loops of I_{ds}-V_{gs} curves of a top-gate transistor, measured in dark (black solid block) and under illumination (red hollow circle), respectively. V_{gs} sweeps from -5 to 3 V and back to -5 V at a sweep rate of 6 V/s. (b) V_{out}-V_{in} dependences for two different top-gate FETs connected in the circuit as depicted in the inset. R is a constant resistor of 100 MΩ. The measurements were conducted at a constant V_{cc}=2.5 V. V_{in} sweeps from -3 to 3 V and back to -3 V at sweeping rates of 6 and -6 V/s, respectively. The solid line is forward and the dash line is backward for each transistor. (c) The schematic configuration of the typical 'AND' and 'OR' circuits design based on two transistors. The inset table summarizes the experimental truth for the two logic gates. (d) A typical switch response from the 'AND' circuit. (e) A typical switch response from the 'OR' circuit, where the final change shows light induced switch on when both the two input are set as logic 0.

FIG. 5.1 a) and b) low and high magnification SEM images of etched Si pattern on a SOI substrate. c) and d) EDX spectra of region (1) and (2) in (b).

FIG. 5.2 An analysis of over-etched Si pattern on a SOI substrate. a) SEM image of a etched Si pad. b) EDX spectra of three typical regions in (a), correspondingly. c) and d) height determination by AFM analysis of the over-etched Si pattern.

FIG. 5.3. a) Low magnification SEM image of crossed junctions in pattern. b) One unit in the pattern. The three white rectangles in the picture are the crossed nanojunctions regions. c)-f) Different density states of CdSe:In NWs over one Si finger in the crossed nano-junctions regions as the white rectangles show in b).

FIG. 5.4 Two typical I-V response of the fabricated diodes, which can be classified into two kinds: a) the turn-on voltage is around 1.5V (ranging from 0.5V to 2V); b) the turn-on voltage is over 5V, from 5V to 8V.

FIG. 5.5 Gate dependent I-V characteristics of a crossed nano-junction FET. a) The gate voltage for each I-V curve is indicated (0, -0.5, -1, -1.5, -2V). The inset picture shows the nano-junction between single CdSe:In NW (red) and individual etched Si NR (blue) schematically. b) Typical transfer characteristics of the nano-junction FET, with a drain bias of 0.5V. The inset is simplified geometry of the crossed nano-junction FET. c) Hysteresis loops of the nano-junction FET at a sweeping rate of 6V/s.

FIG. 6.1. The morphology evolution as indium concentration increases, which depends on the partial vapor pressure of indium, or indium source evaporation temperature. a) and b) low and high SEM images of Sample ZIS-0 with no indium; c) and d) Sample ZIS-1 with indium source evaporation temperature of 500 ^{o}C; e) and f) Sample ZIS-2 (600 ^{o}C); g) and h) Sample ZIS-3 (700 ^{o}C); i) and j) Sample ZIS-4 (800 ^{o}C); k) and l) Sample ZIS-5 (1000 ^{o}C). The inset pictures in color are corresponding to each sample.

List of tables

List of symbols and abbreviations

RT	room temperature
CIS	copper indium selenide
R-G-B	red-green-blue
LED	light emission diode
HF	Hartree-Fock
LCAO	linear combination of atomic orbital
PL	photoluminescence
D^0X	donor related exciton
A^0X	acceptor related exciton
DAP	donor-acceptor pair
LO	longitude optical
QD	quantum dot
FLN	fluorescence line narrowing
1D	one dimensional
NW	nanowire
Δ_{ST}	resonant Stokes shift
VLS	vapor liquid solid
SLS	solution liquid solid
NP	nanoparticle
SFLS	supercritical fluid liquid solid
TOPO	trioctylphosphine oxide
AAO	anode alumina oxide
TOP	trioctylphosphine
PPV	poly phenylene vinylene
ITO	indium tin oxide
EL	electroluminscence
NR	nanoribbon
FET	field effect transistor
ODMR	optical detected magnetic resonance

EPR	electronic paramagnetic resonance
DLTS	deep level transient spectroscopy
D^+X	ionized donor related exciton
A^+X	ionized acceptor related exciton
CBM	conductive band minimum or Ec
E_g	band gap energy
E_F	Fermi level
$E_{form.}$	formation energy of defects
PPC	persistent photo-conductivity
EXAFS	extended X-ray absorption fine structure
PAC	Perturbed angular correlation
MOCVD	metal-organic chemical vapor deposition
MBE	molecular beam epitaxial
JFET	junction field effect transistor
CVD	chemical vapor deposition
SEM	scanning electron microscopy
XRD	X-ray diffraction
TEM	transmission electron microscopy
HRTEM	high resolution TEM
EELS	electron energy loss spectroscopy
EDS	energy dispersive X-ray spectroscopy
XPS	X-ray photoelectron spectroscopy
ICS	intrinsic CdSe
CIS	indium doped CdSe
I_{ds}	drain current
V_{ds}	drain voltage
V_g or V_{gs}	gate voltage
CNT	carbon nanotube
TFT	thin film transistor
MOSFET	metal oxide semiconductor field effect transistor
SAED	selected area electron diffraction

PET	polyethylene terephthalate
NWFET	nanowire based field effect transistor
V_{th}	threshold voltage
μ_{eff}	field effect mobility
V_{fb}	flat band voltage
CMOS	complementary metal oxide semiconductor
SOI	semiconductor on insulator
RIE	reactive ion etching
AC	alternating current
CCD	charge coupled device
DC	direct current
S-D	source-drain
CW	continuous wave
UV	ultra-violet
ZIS	indium doped ZnSe
JCPDS	Joint Committee on Powder Diffraction Standard
V_{Zn}	zinc vacancy

Table of Contents